IN THE UNITED STATES DISTRICT COURT

FOR THE WESTERN DISTRICT OF TEXAS

WACO DIVISION

VLSI TECHNOLOGY LLC	*	
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	*	
VS.	*	CIVIL ACTION NO. AU-19-CV-977
	*	
INTEL CORPORATION	*	December 12, 2019

BEFORE THE HONORABLE ALAN D ALBRIGHT, JUDGE PRESIDING
MARKMAN HEARING

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07:47 (December 12, 2019, 9:05 a.m.)

09:05 THE BAILIFF: All rise.

09:05 (Call to Order of the Court)

09:05 DEPUTY CLERK: Markman hearing in Civil Action Austin 19-CV-977, styled VLSI Technology, LLC vs. Intel Corporation.

09:06 THE COURT: Good morning, ladies and gentlemen. If you would be so kind as to introduce yourself and tell me everyone who will be speaking.

09:06 Mr. Mann, good morning.

09:06 MR. MANN: Good morning, Your Honor. Mark Mann on behalf of VLSI, and, Your Honor, we have a number of lawyers here. Ben Hattenbach, Dominik Slusarzyk. I think that's Smith in Polish. Amy Proctor, Charlotte Wen, Justin Allen, Brian Weissenberg, Andy Tindel, and Morgan Chu who is in trial, Your Honor. So he could not be here.

09:06 THE COURT: Understood.

09:06 MR. MANN: And we're ready to proceed.

09:06 THE COURT: Mr. Ravel?

09:06 MR. RAVEL: Your Honor, Steve Ravel for Intel Corporation. Taking terms today will be Bill Lee who I've already had the honor of introducing to you. Mindy Sooter.

09:06 MS SOOTER: Good morning, Your Honor.

09:06 MR. RAVEL: Joe Mueller and myself. Also on the team is our client in from Santa Clara Ms. Mashood Rassam. Other lawyers are of course Professor James E. Wren III who needs no

introduction. Louis Tompros, Lauren Fletcher and Kate Saxton.

THE COURT: Good to be here.

So let me tell you what I've done. First I want to thank my law clerk who has I don't think slept in the last week just over the sheer excitement of getting to be here at this hearing. The briefs were outstanding. We have both read them. The tutorials are outstanding. I've looked through those already as well. I think in fact yesterday we sent you -- we -- you know, we told you we had an issue with one of the claims. So we are very up to speed and have read everything. It's -- maybe it's at least up with the best drafting of briefs that we've had by far and so it's been very helpful.

So what I guess we should start with is, Mr. Mann, if you would like to put on your tutorial, that would be great. Or whoever's going to do it.

MR. MANN: Your Honor, I think we understood, and we can -- I'm sure we can do it either way, but we're going to do maybe a mini tutorial for each patent. Is that what we planned on doing?

THE COURT: Yes, sir.

MR. MANN: So I think Mr. Hattenbach maybe has -- Amy Proctor has the first term, Your Honor.

THE COURT: Okay.

MR. RAVEL: For housekeeping, Judge, in that regard, subject to the way you want to do it, the parties had thought

09:08 we would just go down through the order of the joint claim
09:08 construction statement claim by claim.
09:08 THE COURT: That's the way I'm prepared to do it.
09:08 MR. RAVEL: Okay.
09:08 THE COURT: And just for the record, if we're -- if I'm
09:08 correct, what we're starting off with is the '522 patent, and
09:09 it would be regulate/regulating at least one supply from a
09:09 power source and an inductance.
09:09 MS. PROCTOR: That's my understanding as well, Your Honor.
09:09 THE COURT: Very good.
09:09 MS. PROCTOR: Amy Proctor for VLSI.
09:09 Well, so, Your Honor, I believe you have a copy of the
09:09 slides. If you don't, we can certainly pass one up to you.
09:09 THE COURT: Is it what I've already seen? I think I've
09:09 got a copy.
09:09 MS. PROCTOR: So we have a fresh set of slides that
09:09 include our slides for the argument and also some of the same
09:09 tutorial slides and a little bit --
09:09 THE COURT: You can never have too many slides.
09:09 MS. PROCTOR: I'll get you a hard copy right now.
09:09 All right. There we go. We got the screen working too.
09:10 So can you jump to Slide 16, please?
09:10 Thank you.
09:10 All right. So the '522 patent. So this patent was filed
09:10 in November 2000.

MR. RAVEL: Do you have a copy of your slides for us?

MS. PROCTOR: Sure.

(Conference between counsel.)

MS. PROCTOR: Thank you.

So the '522 patent developed and filed back in November 2000 identified a need for a method and apparatus that could adjust the system clock and/or the supply voltage based on a couple of things. So the application actually being performed and also the processing capabilities of the circuit. And the goal here was to conserve power. And so exactly what the inventors found is that you can do this. If you take into account the actual processing needs of the application, including if there are multiple applications running, you can look at what those applications actually need in terms of their clock frequency and you can adjust that and then you can also adjust the voltage. And by adjusting the voltage so that you're not always operating at the maximum voltage you might ever need but instead you're operating at a lower voltage when you don't need that maximum amount, --

THE COURT: And you can go up.

MS. PROCTOR: -- you can save power.

THE COURT: Right? And you can go up?

MS. PROCTOR: Right. You can go up when you need to and down.

So one way to implement a system that can do this is to

use a converter. And we talked on -- about this a little bit in the tutorial, but there are a number of different types of converters that can be used to convert input power to a power level that's better suited to the system.

And there are a couple of examples. This is actually a slide in Intel's tutorial and you'll see they provided this exhibit DX18 that shows five different types of converters. And what they focused on were just the first two. So they told you a lot about buck converters and boost converters, but if you actually look at their reference here, it goes through a number of others as well, including one that we talked about in our tutorial. So the very next one on this list from Intel's reference here is a buck boost converter. And so this is a converter where it's -- this is an example of one at least. And so in this simple example what you have is you have an inductor being powered by the power source when the switch is closed. So that switch at the top. And then when the switch is open, that inductor is then connected to power the load. So you store some amount of energy in the inductor and then you can actually provide that to the load. And so you can go back and forth between these two modes where you're charging the inductor or discharging the inductor, and that determines how much power you actually provide to the load. So in this configuration you can either provide more. So it -- also the input is five volts. If you charge up the inductor enough, you

could actually provide more than that. You could provide six volts to the load. Now, if you charge the inductor less for a shorter amount of time, you could provide a lower amount. You could provide four volts. So it's a very flexible configuration that allows you to provide different voltage levels to the load.

And of course there are many other types of converters as well. So one more we mentioned, in Dr. Conte's explanation was the flyback converter, and this is actually also discussed in Intel's reference DX18, and it's similar to the buck boost, but instead of having a direct coupling where the inductor is actually where you have a single inductor that's part of the full circuit, you have this magnetic coupling between two inductors. So it works in a very similar way. The switch could be where it's shown down here. It could also be where we've just shown on the last example at the top and you can do kind of the same thing here where you can charge up an inductor and then use that inductor to provide voltage to a load. But here of course there's no direct electrical connection. So these are just some examples of types of converters that could be used in a circuit that can achieve the goals of the '522 patent.

And the '522 patent itself is pretty clear. So it embraces this flexibility. It says in the specification a buck converter may be -- there's a missing here -- may be used

instead of a boost convert or a combination of a buck and boost converter may be used. The buck boost example is a combination. This is straight from the spec of the original patent. So this demonstrates the patent's flexibility.

Now, you might have heard a little bit from Intel about Figure 1 in the patent, and this is -- these are their labels on Figure 1. They say power source, inductance, regulating circuitry, and they describe this as a boost converter, but the patent is very clear this is just one embodiment. And I know Your Honor is very familiar with basic claim construction law that says the illustration of a specific embodiment does not limit the claim language. And, by the way, Intel doesn't ever really argue that it does. So we'll get to that in a minute, but I think the parties agree here there are a number of different converters that can be used in this type of circuit.

So the actual claim term here, regulate or regulating at least one supply from a power source and inductance. It appears, for example, in Claim 1 and throughout a number of the other claims. So Your Honor has our proposed instructions. We propose plain and ordinary meaning and Intel has proposed this paragraph on the right here. And what these two proposals show is that no construction is necessary. So it's very clear that both parties have maintained every single word of the claim language and proposed maintaining that. And so you can see on the right here we've kind of marked up the words Intel's added

09:16 in red, and if you count, it's 14 words they're trying to add
09:16 to the claim, but everyone agrees that the words in the
09:16 claim -- Intel reuses each and every single one of them. The
09:16 words in the claim are understandable and do not require
09:16 further explanation. And so when that's the case, it's really
09:16 a simple situation for Your Honor. The claim just simply does
09:16 not require definition. And the law on this is also very
09:16 clear, for example, in Renishaw. The Federal Circuit has
09:16 explained that a claim must explicitly recite a term in the
09:16 definition before a definition may enter the claim from the
09:16 written description. And there are plenty of examples also of
09:16 district courts addressing this, including the Eastern District
09:16 of Texas, explaining that where the parties propose repeating
09:16 the language of the claims in their constructions, then you
09:16 really don't need to do any more here and you can stick with
09:16 those same words.
09:17 So what Intel's construction does is it tries to add two
09:17 non claimed limitations. So it's really a rewriting of the
09:17 claim. And here's an example. It's a little confusing of what
09:17 they're trying to do. So they're moving some words around.
09:17 They're inserting other words, and what they've come up with is
09:17 a whole new set of language for the claims that adds two
09:17 separate limitations: One, that the inductance be connected to
09:17 a power source, and, two, that the inductance be positioned
09:17 between the power source and the regulating circuitry.

09:17 Now, I know Your Honor knows that generally speaking we don't just add limitations to claims. Of course it's over a century of law saying that if we want to begin to include elements not mentioned in the claim to limit the claim we should never know where to stop. So this just on its face violates kind of foundational principles of claim construction. The patent doesn't support these new limitations. There's no requirement on the connection in the patent. There's no requirement on the specific placement that Intel wants in the patent. And, in fact, Intel agrees. So Intel has not argued and doesn't rely on the patent to add these limitations. Intel's relying only on the re-examination history, which I'll get to in a moment.

09:18 And, actually, worse than just being unsupported by the patent, Intel's construction actually contradicts the specification. So we looked, for example, earlier at this excerpt from the specification explaining that a buck converter may be used or a combination of a buck and boost converter. And Intel has described its own construction -- this is from its opening brief -- as requiring a boost regulator configuration. So Intel's designed its construction in an attempt to exclude all other types of converters, and that's Intel's own position. I think in their reply they came back and said, oh, maybe there's something that's a boost regulator that has some extra component, but this is their position, that

09:19 only boost regulators satisfy their construction, and it's just not supported by the patent and it's not supported. It actually contradicts the specification.

So really absent any exceptions to the foundational rules of claim construction, we're done. It's very clear here that the parties agree the claim terms are understandable and that the foundational rule of applying plain and ordinary meaning should apply. Now the burden really shifts to Intel. Intel wants to invoke the re-examination history to argue that we should rewrite the claim according to its kind of interpretation of that re-exam history to add these two new limitations, and it's just not warranted by that history.

So there's an incredibly high standard for disclaimer. And, again, this is Intel's burden to show that the statements made during re-examination or the prosecution history are both clear and unmistakable. We have -- the Federal Circuit has said we have consistently rejected prosecution statements too vague or ambiguous to qualify as a disavowal of claim scope. And there's a very good reason for this extremely high standard. We really only rewrite claims in a couple of very narrow situations, because if we start doing it more broadly, more generally, it really does trample on the prosecution process. Claims are very carefully drafted and reviewed and it just would violate a number of foundational principles of claim construction to routinely rewrite claims in the way Intel

09:20 proposes. So there are really a couple of only very narrow
09:20 circumstances where you can do that. One is, for example, if
09:20 the inventor provides an express definition, and it makes sense
09:20 there because you have extremely clear guidance on how to
09:20 define the term. The inventor spelled it out for you in some
09:20 way that's very clear. So that's one. And another one is if
09:21 there's disclaimer but only if that disclaimer is so clear and
09:21 unmistakable and definitional that it's even possible to come
09:21 up with a construction that is fair and reasonable and that
09:21 it's clear enough to trump the whole rest of claim construction
09:21 jurisprudence.
09:21 So if we go through the re-exam history, I have a slide
09:21 with each circuit. I'm happy to look at any of them Your
09:21 Honor's interested in, but they are all pretty similar. So
09:21 what happens is there's this -- I've tried to excerpt on these
09:21 slides and you'll see there's a -- like I said, a series of
09:21 them. I've tried to excerpt the key discussion of each of the
09:21 prior art circuits for you. And what the patent -- what the
09:21 patentee said were things like -- this is the first one that
09:21 comes up, Dancy. Dancy does not regulate at least one supply
09:21 from a power source and an inductance, and here's the full
09:21 explanation for why. Because the power supply control signal
09:21 operates switches S1 and S2 from the power source Vin alone.
09:22 So that's what we have to work with. Really not clear exactly
09:22 what or why the circuit's being distinguished, and I'll get

into that a little bit more later what some other interpretations are here, but that's kind of the full statement we have on this.

So another example is Gutnik II, and here the patentee described the circuit. So it explains that it's implementing with a PWM controller, driver, inductor, capacitor, and then made a very similar statement: Does not disclose regulating Vout from a power source and an inductance.

So, again, some of this I think is just clearly background just describing the circuit and then the circuit's printed there and then there's just this kind of conclusion that it does not disclose something.

And then actually if you go on right below the figure, what the patentee said about Gutnik II was that it uses the LC filter in a buck configuration but doesn't regulate as the claim requires. So this actually signals to me that the patentee intended to include buck configurations, but, again, we really don't have much guidance here on why these circuits are being distinguished.

So six more of these we can look at, but they really are pretty consistent in how they just repeat claim language and say the prior art does not disclose the term. And so these are on Slides 46, 47, 48 all the way through 51.

And so what the Federal Circuit has said is that you actually can distinguish prior art during re-exam during the

prosecution without constraining the definition of the claim term as being argued, and so that's really what we think is happening here. There was some distinguishing. We don't dispute that, but Intel here bears the burden of showing that the patentee limited the claims to Intel's proposed construction clearly and unmistakably, and I just don't see that here in this record.

So if we kind of look at this history and ask ourselves some questions, what's the patentee's basis for distinguishing? We have a little bit of guidance that we saw in those slides, but there really are multiple reasonable interpretations.

What specific feature is the patent focused on differentiating? Not clear. And then this is really the critical question. Should the claim be defined differently based on those statements and how? And we just don't have that here. This record has no affirmative defining statements. It never tells us clearly and unmistakably that the inductance has to be both connected to the power source and located between the power source and the regulating circuitry. So that's really the issue. The patentee's statements are silent on the location of the inductance, and it's just really not clear. I believe that they're limiting the definition in that way.

And so on Slide 54 there are other reasonable interpretations. So it seems like in Dancy the patentee's distinguishing the power supply control signal and I would say

basically every discussion it seems like the patentee is just providing background on some of these circuits and that background does come up later. The patentee later makes arguments talking about why it wouldn't have been obvious to combine these circuits with Clark '086 in part based on the fact that they aren't suitable for integration and things like that. So some of this background on the circuits really is just foundation for later arguments. And, in fact, even the fact that those circuits are buck -- include buck configurations is background for arguments on Claims 23 and 29 where the patentee actually added claims during the re-exam that would require the ability to increase or decrease the voltage, and I have Claim 23. I'll show you that in a second. So a lot of that really was just background for later arguments the patentee wanted to make. And there's also -- it's also very possible that the patentee was commenting on the relationship between the inductance and the regulating circuitry. So I'll give a quick example going back to the buck boost configuration on that.

So, again, where the alleged disavowal is ambiguous or open to multiple reasonable interpretations, it just doesn't rise to the standard for prosecution disclaimer. And this has comes up in cases, plenty of cases. We have one example here on Slide 56. And what happened here was the -- in the -- the patentee made statements that said, using a server through a

centralized interface is contrary to the claim limitations. So a pretty clear distinguishing statement. So the district court relied on that to find that the storage units cannot be centrally controlled, and the Federal Circuit said, no. It kind of went too far. The district court read more into the patentee's words than were clearly there, and that's what we think Intel's doing here.

So what the patentee has really just said references do not disclose some element, that is not the same as affirmatively requiring the two limitations that Intel's added. It's just not there. And, in fact, I can demonstrate this with an example. So not only is it just not clear and unmistakable because there is no -- you can't draw this connection. Intel's actually wrong. Its construction is just too narrow and it's contradicted not only by the patent but by the re-examination history.

So like we talked about before, there are many possible converters. So I've shown here the buck boost again, a flyback converter and many others that the patentee never distinguished during re-examination and actually explicitly says in the spec may be used.

But the buck boost example actually may not satisfy Intel's construction. I think first of all Intel has said it wouldn't satisfy Intel's construction because Intel has said its construction is limited to boost configurations, but, also,

09:28 if we look at -- just look at the way the circuit's arranged, especially the requirement that the inductor be between the power source and the regulating circuitry, it's just not there. If the current is flowing clockwise here, the inductor is not between the power source and the regulating circuitry, but this is clearly something that should fall within the scope of the claims both before and after the re-examination.

And I mention Claim 23. This is a claim that was added during re-examination and it actually requires that the power supply control signal provide the at least one supply selectively at a voltage greater than or less than a voltage of the power source. So we have a dependant claim depending from Claim 1 that says you have to be able to provide voltage that's either higher or lower than that input power source voltage, and Intel has said under its construction boost only. So Intel has said basically if you adopt its construction, this claim that was added during re-examination. So therefore clearly the examiner and the patentee believed were fully consistent with statements made during re-examination. This claim would no longer even be possible to satisfy -- Claim 1 would be narrower than this dependent Claim 23.

Intel tries to kind of avoid this -- these issues with its proposal saying, well, it's not fair. It's not fair for the patentee to have used this one definition when it was arguing validity and now to try to argue it for a different definition,

09:30 but, first of all, Intel's never argued that the patentee
09:30 actually made inconsistent statements here on infringement and
09:30 validity. And what would really be unfair, we think, is to
09:30 limit the claims based on Intel's after the fact
09:30 misinterpretation of ambiguous statements to exclude whole
09:30 dependent claims from even being possible to be met based on
09:30 assumptions and guesses about what the patentee meant.
09:30 And if Your Honor's concerned, oh, maybe these claims
09:30 never would have survived re-exam if we hadn't made this
09:30 argument, if the patentee hadn't said this, that, I don't
09:30 think, has support either because the patentee made multiple
09:30 arguments during re-examination. Each of these circuits
09:30 appeared as part of an obviousness combination and the patentee
09:30 explained in each case why it would not have been obvious to
09:30 make that combination and why there was actually teaching a way
09:30 in what was identified as the primary reference from the
09:30 combination. So there's also no real fairness concern there.
09:30 On Slide 63 I just have this one quick example of kind of
09:31 the dangers of rewriting claims after the fact without clear
09:31 guidance from the inventor and from the patentee. Intel's
09:31 construction really doesn't make things more clear. So this is
09:31 Intel's own picture on the left here from Intel's brief. It
09:31 has labeled what it believes to be the regulating circuitry and
09:31 the inductance and the power source, and Intel's construction
09:31 requires that the inductance be between the power source and

09:31 1 the regulating circuitry. Well, how can you assess that when
09:31 2 Intel's kind of dropped the inductance here in the middle of
09:31 3 what it's called the regulating circuitry, right? So I think
09:31 4 there's also just a practical problem of -- so we have kind of
09:31 5 two problems with going down this path of using the
09:31 6 re-examination to rewrite the claims. There's the legal issue
09:31 7 of when it's not clear and unmistakable, it really should not
09:31 8 trump every other foundational claim construction principle,
09:31 9 but also there's a practical problem. If you don't have enough
09:32 10 clarity from the patentee or from the inventor on how to write
09:32 11 the claims after the fact, then you end up just creating more
09:32 12 confusion instead of more clarity.
09:32 13 So, ultimately, plain and ordinary meaning really is the
09:32 14 only appropriate construction here. The parties agree that
09:32 15 every word in the claim is understandable to a person of
09:32 16 ordinary skill in the art, and these re-examination statements
09:32 17 simply do not have the clarity necessary to be definitional.
09:32 18 And so it just isn't fair to the patentee. It isn't right to
09:32 19 rewrite the claims based on assumptions and guesses about what
09:32 20 the patentee meant in the way that actually contradicts both
09:32 21 the patent and the rest of the re-examination history and even
09:32 22 amended -- I'm sorry -- added claims during re-exam.
09:32 23 THE COURT: Thank you very much.
09:33 24 MR. MUELLER: Good morning, Your Honor. My name is Joe
09:33 25 Mueller.

09:33 THE COURT: Mr. Mueller, good morning.

09:33 MR. MUELLER: May I pass out some hard copies for you?

09:33 THE COURT: Of course.

09:33 MR. MUELLER: So if I could, Your Honor, I'd like to start with a brief review of some tutorial slides that we prepared. I'll go through some of them rather quickly in the interest of cutting to the core issues before Your Honor today. May I proceed?

09:33 THE COURT: Absolutely.

09:33 MR. MUELLER: So first there's some basic concepts on current voltage and inductors, and these I'll just sort of breeze through because I'm sure Your Honor's familiar with the basics, but this patent involves consideration of the ways in which voltage is converted or adjusted within certain types of circuits.

09:33 And fundamentally we have current, the flow of electrons, voltage, the pressure in the circuit. And of particular relevance to this patent is the circuit element of an inductor or an inductor coil. And those create magnetic fields. When current runs through them, those magnetic fields serve as storage tanks for energy, converts electrical energy into magnetic energy. And there's several beneficial effects of that physics concept, the concept of the magnetic field being created. It can serve to slow down current in certain circumstances and it can serve to add current in others

depending on whether the storage vessel, this magnetic field, is being created or collapsed. Now, when it's created, it takes the current flowing into it and converts that electrical energy into magnetic energy, and when the magnetic field collapses, it's converted back into electrical energy and current flows out of the coil. And so those are the basics for inductor coils. And you can see it here. There's a five volt input that generates the magnetic field converting some portion of the electrical energy into magnetic energy, slowing down the current. When the voltage is shut off, the magnetic field collapses and current is released from that storage vessel.

And that takes us to the next building block here from a technical perspective switching regulators. And these, as the name suggests, are switches used to regulate certain circuitry. And in this context, the context of power converters, these switches are used to regulate voltage. So here, and Ms. Proctor showed you this earlier, is an example of two different types of power converters, a buck converter and a boost converter. And I want to pause here, Your Honor, to make a point that I'm going to come back to a few times, which is that the labels "buck" and "boost" are really not what's critical here. They're useful labels. They are used in the field to refer to certain configuration of circuitry, and that's why we use them in our tutorial and we use them in our brief. But what really matters at the end of the day is what's claimed in

09:36 the particular patent claim term at issue and how that
09:36 corresponds to certain circuit elements. So I'll explain that
09:36 further when I come back to it in a bit, but I do want to make
09:36 that threshold point these are useful labels. They're labels
09:36 that are used in the field, but at the end of the day, the
09:36 claim language governs.
09:36 And here we have a buck converter at the top and a boost
09:36 converter at the bottom. And, Your Honor, may I approach the
09:36 screen?
09:36 THE COURT: Oh, sure. Y'all don't need to -- y'all are
09:36 free to move about in here.
09:36 MR. MUELLER: Thank you, Your Honor.
09:36 So here we have an input source of voltage and we see the
09:36 regulating circuitry in blue. There's a diode here which just
09:36 forces current in a single direction, the direction of the
09:36 arrow. And then we have an inductor, that magnetic coil on the
09:36 right-hand side. And of particular relevance to the dispute
09:36 before Your Honor, the regulating circuitry here is before the
09:37 inductor. It's located physically prior to the inductor. So
09:37 we have a power source, then regulating circuitry and then an
09:37 inductor. And another way to put it is the regulator is
09:37 regulating from a power source here but not regulating from an
09:37 inductor. There's no inductor before the regulating circuitry
09:37 takes operation.
09:37 If we switch down to the boost converter, it's a different

configuration. And here we have the regulating circuitry in the center of the diagram. We have that diode in the top right-hand corner. We have the power source and we have the inductor. And here the power source is connected to the inductor, and the regulating circuitry is downstream from the inductor. It's a critical distinction between the buck converter and the boost converter. It's downstream from the inductor. So here again we have regulating circuitry in both, but in the bottom boost converter it's regulating from not only the power source but also regulating from the inductor. It's regulating from both.

So if we talk about how these work in operation, and we'll start with the boost converter, again, the inductor is connected to the power source and positioned between the power source and the regulating circuitry. It's regulating from the inductance and the power source. The boost converter, the inductance is located on the output of the regulating circuitry. The regulating circuitry is only regulating from the power source alone. And that distinction makes a difference. So here's the boost converter in operation. And when the switch is closed -- this is a regulating circuitry. When the switch is closed, current flows through this circuit. This storage vessel is charged up, that magnetic field is created, and when the switch is opened -- so here you can just see the magnetic field being created, electrical energy being

09:39 stored in the form of magnetic energy and that inductance coil. When the switch is open, now the pathway for current changes and it's going to flow through that diode. And here we have actually two sources of voltage that are being combined. We have the input voltage over here, but then remember we had this storage vessel that had been charged up. Now it's going to discharge and so we have two sources of voltage, the input voltage and the additional boost from this inductance coil, this magnetic field releasing that energy. And the combined energy is higher voltage than the input voltage. It's been boosted by virtue of the magnetic field releasing that energy.

I'll try to skip ahead here to the buck converter. Okay. So we have the buck converter. And as a threshold matter, if you had a circuit that looks like this one, Your Honor, where we have the input voltage, a regulating circuit and then some load, it could be almost anything, a lightbulb or something that will consume the energy on the other side. In the abstract without a buck converter, the input voltage will flow through this circuit when the regulating circuit is closed and so the voltage will jump from zero to the input voltage level. If we shut off the regulating circuit or open it, I should say, the voltage will shut off and we drop down to zero again. And each time we turn the circuit on or off, we will jump up or jump down from the input voltage to zero or vice versa, and what we see as a result is a square wave, a very choppy current

jumping from zero to the top voltage and back again.

THE COURT: And that was on Slide 21?

MR. MUELLER: That's right, Your Honor. That's Slide 21. That's Slide 21.

So the buck converter looks like this, and this is what we looked at earlier. We have here this regulating circuit. We have the regulating circuit right here. There's a diode. There's an inductor downstream, downstream from the regulating circuitry. And what happens is the input voltage comes in, goes into the inductor coil which starts to build up that magnetic field, and that tends to reduce the voltage because a portion of the electrical energy that have flowed into the inductor is converted into a magnetic field and so therefore the current that flows out is lower. It's the difference between a storage vessel that has not yet been filled up in this circumstance. So it's going to be filling itself up with the current from the input voltage as distinct from the boost converter. You recall it was fully filled up in that stage one. Then it was released. Here it hasn't been filled up yet so it's drawing energy from the current, and that serves to lower the voltage as compared to what the input voltage was over here. It's reducing it. So rather than boosting it, it's reducing it.

THE COURT: And that was Slide 22?

MR. MUELLER: That's Slide 22 into 23, Your Honor, right

here when we open it up.

Now, when the switch is open, recall that in the absence of this inductor coil, we would go all the way down to zero, but here when the switch is open, that storage vessel now will release the current that it has stored in the form of magnetic energy. That magnetic field will collapse and some current will be released. Now, it won't be as much as the input voltage. It'll be somewhere in between, but basically what we have is the presence of the inductor coil lowering the input voltage when the circuit is closed and then raising the current when the circuit is open because it's releasing the energy that had been stored in the form of magnetic energy.

And so, Your Honor, rather than that square wave that we had earlier, it's a bit of a smoother flow of current over time. It's not as high as it would have been in the absence of the inductance coil because that magnetic field draws off some of the current when the circuit is in operation, but then rather than going to zero, it goes to a bit above zero because the magnetic field will release energy once the switch is opened up and the input voltage is no longer being applied. So it's a more smooth flow than the square wave that we had in the absence of the inductor coil, and engineers find that useful for certain types of circuitry. So therefore these buck converters can serve useful purposes for some applications.

THE COURT: So we can find that on 29 and 30?

09:44 MR. MUELLER: Those are Slides 29 and 30, Your Honor. That's right.

09:44 So Slide 31 here we have a summary of what we've just gone through. For a boost converter the output voltage is higher voltage than input because in Stage 1 we have the magnetic field charged up, and then in Stage 2 it's released along with the input voltage to create that boost. The inductor's position is connected to the power source and between the power source and regulating circuitry. So in this instance the regulation is from, regulating a supply from the power source and the inductor coil and it adds extra energy.

09:44 The buck converter lower voltage than input, meaning when you have the voltage applied, the inductor will draw off some of it as that magnetic field is created, but then once the voltage is no longer being applied, it will release that energy to create that smoother flow over time. It's located at the output of the regulating circuitry. So here the regulation is from the power source alone. It's not from the power source and the inductor, and, again, the purpose of this circuit here in perspective is to smooth out the current over time.

09:45 And, again, that's Slide 31, Your Honor.

09:45 So with that in mind, Your Honor, if we could turn to the patent background, in Slide 33 here we just have the cover page. This is a method and apparatus for controlling power consumption of integrated circuit, and as Ms. Proctor said, the

09:45 valid purpose of the patent is to have a more efficient
09:45 approach to power consumption by circuits in view of the
09:45 purpose of the circuit and also the application that might be
09:45 running on it. That's the goal of the patent.
09:46 Here's Figure 1 on Slide 34, Your Honor, and this shows a
09:46 boost converter.
09:46 We have a power source. We have an inductance. We have
09:46 regulating circuitry. This is Slide 35. There's no dispute
09:46 that these are in fact what I have labeled them as. So we have
09:46 a power source here. We have an inductance and we have
09:46 regulating circuitry, and in this particular embodiment the
09:46 regulation is from the inductance in the power source, and that
09:46 is the circuit shown in Figure 1.
09:46 Now, before I leave the tutorial and move to the Markman
09:46 slides, Mr. Lee, if you could just pull up the patent and if
09:46 you'd please go to Column 6, Lines 53 to 55.
09:46 Your Honor, you were told a few times that there's an
09:46 embodiment in the patent that involves a buck converter, and it
09:47 absolutely correct that a buck converter is mentioned, but I
09:47 did want to highlight exactly where it's mentioned.
09:47 If you could just zoom back out, Mr. Lee.
09:47 This is the last paragraph of the specification.
09:47 If we start with the preceding discussion, Mr. Lee.
09:47 The last paragraph before the claims and the very last
09:47 sentence of the last paragraph it says: For example, a buck

converter may be instead of a boost converter or a combination of a buck and boost converter may be used. There's no electrical diagram of any circuit that would meet that depicted anywhere else in the specification. It's this one sentence. And so the question is, is this sentence, along with the claim language and the statements and re-examination, sufficient to define the claim in a way that would cover a circuit configuration that involves a buck converter? And the answer, as I will explain, Your Honor, is no, but I did want to put in context that sentence. There's no actual circuit design depicted in this patent that shows how the invention could be used. There is in fact a sentence, but it is that sentence alone.

So if you could go over to the Markman deck, Mr. Lee.

Your Honor, this is the term at issue here, and this is Slide 3. Regulate at least one supply from a power source and an inductance. Regulate at least one supply from a power source and an inductance.

Our position, Your Honor, is, from means the power source and the inductance or before the regulating circuitry. That's as simple as that. That is our position, and our position is that any doubt on that issue was confirmed by not one, not two, not three, but eight statements during examination with respect to -- actually more than eight statements. Eight prior art references and the applicants' distinctions of those references

09:48 made abundantly clear that from a power source and an
09:49 inductance meant from a power source and inductance upstream of
09:49 a regulating circuitry. So I mentioned at the outset, Your
09:49 Honor, that the label "buck and boost" at the end of the day is
09:49 not the key. The key is what is claimed. The buck and boost
09:49 concepts, again, are industry terms and they are useful terms.
09:49 What really matters here, though, is, what does this mean?
09:49 Regulate at least one supply from, the power source and an
09:49 inductance. And our position, Your Honor, is that from means
09:49 before. It comes before the regulating circuitry, and that was
09:49 confirmed over and over and over again during the
09:49 re-examination.
09:49 So our construction is regulate at least one power supply
09:49 from an inductance connected to a power source where the
09:49 inductance is positioned between the power source and the
09:49 regulating circuitry.
09:49 Now, there was arguments made to Your Honor by Ms. Proctor
09:49 that we're adding words, we're trying to rewrite things. We're
09:49 not, Your Honor. What we're trying to do is to hold the patent
09:50 owner to precisely what the patent owner at the time -- it was
09:50 actually a predecessor and interest -- represented to the
09:50 Patent Office during re-examination. And to set the stage for
09:50 this, this was an interparty's re-examination under the pre
09:50 America Invents Act approach to re-examination. It involved a
09:50 predecessor and interest Sigma Tel that was in litigation with

09:50 another company. That other company sought and initiated an
09:50 interparty's re-examination. During that re-examination the
09:50 claims were amended and amended in an important way.
09:50 And, Mr. Lee, if you go the re-examination certificate,
09:50 please.
09:50 So this is the certificate that ultimately issued after
09:50 the re-examination proceeding, Your Honor, and if we could go
09:50 to Column 1 of the re-examination certificate.
09:50 And, Your Honor, if you look at Claim 9, this is at Line
09:50 32 to 34. So the original language in the original patent as
09:51 first issued stated: Regulating at least one supply from, and
09:51 then this language is in the original claim, at least one of:
09:51 A linear regulator and a power source and an inductance based
09:51 on a power source control signal. And this is what's known as
09:51 the Markush format for claim writing where you can pick from a
09:51 series of options to satisfy the claim limitation.
09:51 So regulating at least one power supply from at least one
09:51 of a linear regulator and a power source and an inductance
09:51 based on a power supply control signal. To satisfy that claim
09:51 as originally written, you could have a regulating circuit that
09:51 was regulating at least one supply from any one of those
09:51 things. So this would have been met by regulating circuitry
09:51 that was regulating a linear regulator or a power source or an
09:52 inductance based on power supply. So as originally written,
09:52 this would indeed cover a buck converter as one example because

09:52 that would have a power source before the regulating circuitry. But the claim was amended. It was amended during re-examination. It was amended for good reason. It had to be amended to overcome the eight prior art references the examiner used to reject it, and it was amended by deleting this phrase at least one of a linear regulator and was excised from the claim. That converted it, Your Honor, from a Markush form claim into a claim where there had to be regulation of at least one supply from a power source and an inductance. So it became a required conjunction instead of a series of Markush options.

The required conjunction was a power source and an inductance. Both of those had to be part of what was being regulated from. So the regulation from went from being something that could be met by a whole variety of configurations to something that required in the claim language itself regulation from a power source and an inductance, both of them.

And with that amendment in mind, Your Honor, if you go back to the Markman deck, Mr. Lee.

During this re-examination the examiner rejected the original claim language based on eight prior art buck converters. And there's no dispute that those eight prior art references in fact depict buck converters. I will show you each one of them, Your Honor. Rejected based on eight prior art buck converters. And so the applicants needed to address

09:53 those buck converters including in light of the amended
09:53 language, and they did so again and again and again.
09:53 So let's go through some of them. And the presentation
09:53 from VLSI -- I went through them extremely quickly. I'm going
09:54 to take my time a bit here, Your Honor, to show you precisely
09:54 what the applicants said during this re-examination. Here's
09:54 Slide 7, Your Honor. This is Dancy, one of the regulators.
09:54 And the applicant said that Dancy's regulator does not regulate
09:54 at least one supply from a power source and an inductance.
09:54 That's the required conjunction under the amended claim.
09:54 Because the power supply control signal operates switches S1
09:54 and S2 from the power source alone. From the power source
09:54 alone. Crystal clear under any standard that you could
09:54 conceivably apply to that statement, Your Honor, that they were
09:54 distinguishing a circuit design where regulation occurred from
09:54 the power source alone.
09:54 And then they went on and explained exactly what that
09:54 meant. This is not a mystery or a question mark or any
09:54 ambiguity at all. It is crystal clear. Not from the power
09:54 source and the inductance as recited in Claim 1. What that
09:55 means unequivocally, unmistakably under any conceivable
09:55 standard you can apply here is that the regulating circuitry
09:55 needs to be after both the power source and the inductance.
09:55 That's what it means to regulate from the power source and the
09:55 inductance, and it's not met by a buck converter because the

09:55 1 inductance is downstream.
09:55 2 And here you see, Your Honor, these are the circuit
09:55 3 components. There's no doubt that each one of those are in
09:55 4 fact what I've depicted here. There's no dispute between the
09:55 5 parties as to what they are. There's a power source and a
09:55 6 regulating circuit and a magnetic inductance coil downstream
09:55 7 from the regulating circuitry. What does that mean? It means
09:55 8 the power source alone precedes the regulating circuitry. The
09:55 9 regulation was from the power source alone.
09:55 10 And, again, there were more statements with respect to
09:55 11 Dancy distinguishing on this -- the basis of this precise claim
09:55 12 limitation before Your Honor.
09:55 13 The Wei reference. Same issue. Wei's inductance is not
09:56 14 connected to a power source and Wei does not disclose
09:56 15 regulating from a power source and an inductance. The figure
09:56 16 in Wei was actually labeled buck converter. Labeled "buck
09:56 17 converter." So that one sentence I showed Your Honor at
09:56 18 Column 6, Lines 53 through 55 where there's a reference to buck
09:56 19 converters possibly meeting the claims under some alternative
09:56 20 embodiment, that's before they had to make these statements
09:56 21 during re-examination where they distinguished expressly and
09:56 22 repeatedly buck converter configurations.
09:56 23 Same thing we have regulating circuitry in a power source
09:56 24 and the inductance downstream. The implication of that is that
09:56 25 the regulation is not from a power source and an inductor.

09:56 Min. Exact same issue. The application distinguished on the basis that it did not meet the from a power source in an inductance language.

09:56 Here we see the power source and the regulating circuitry and the inductance was downstream, and Figure 3, the subcaption is simplified schematic for the buck regulator. Prior art reference on its face, Your Honor, said it was a buck regulator, and the applicants distinguished it on that basis. And, again, the label "buck regulator" at the end of the day is not the crucial point. The crucial point is what it is, and what it is is something with an inductance coil downstream, and the applicant made clear that would not meet the claim limitations. That's Slide 13.

09:57 Goodman. Exactly the same issue, Your Honor. Here we have the power source, the regulating circuitry and the inductance downstream. Once again, the applicant italicized the language from a power source and an inductance and said that Goodman did not have it. And also said that -- this is part of the applicant's statement. Goodman's DC/DC converter in fact uses the external LC filter in a synchronous buck configuration. So part of their description of what they said was different was that it was a buck configuration.

09:58 Burd I. Power source regulating circuitry inductance downstream. They said it doesn't meet the from a power source and an inductance language. And then they further said that

09:58 the DC to DC converter in fact uses the external LC filter in a
09:58 synchronous buck configuration.
09:58 Burd II, same thing. Power source regulating circuitry
09:58 downstream inductance. Once again, the applicant said that did
09:58 not meet the language from a power source and an inductance,
09:58 and they further stated that this converter was a buck
09:58 configuration.
09:58 Gutnik I, same thing. Power source regulating circuitry
09:58 and inductance. Gutnik I discloses a buck converter in the
09:58 words of the patent applicant, and that's different because of
09:59 the from a power source and inductance claim language.
09:59 Gutnik II, same thing. Power source regulating circuitry
09:59 and inductance. Applicant told the Patent Office this is a
09:59 buck configuration, distinguished it from their claims on the
09:59 basis of the italicized language from a power source and an
09:59 inductance.
09:59 Now, Your Honor, you were told that there's no real way to
09:59 know what the applicants meant. It's a bit of a mystery.
09:59 There's multiple possible interpretations. It's not a mystery
09:59 when you take your time and you look at what they actually
09:59 said. If you look at what they actually said over and over and
09:59 over again, the italicized, the claim language that we're
09:59 focused on now, they distinguished it on the exact precise
09:59 basis that we are advocating that Your Honor hold them to now.
09:59 There's no doubt. There's no mystery. There's no confusion if

09:59 you look at what they actually said over and over and over again.

So those are the representations they made, Your Honor, and those are in our slide deck through Slide 19.

What I would say, Your Honor, is that the reason why we think this is important and why we think that the construction that we've asked Your Honor for --

And, Mr. Lee, if you'd jump to the summary of the proposed constructions.

The reason why it's significant, Your Honor, is because the jury needs to know exactly what this means from an inductance and a power source. The claim language says regulating at least one supply from a power source and inductance. That's the phrase they italicized when they were discussing the prior art with the examiner over and over again, and what the jury needs to know is that that means the inductance needs to come before the regulating circuitry, and we've tried to capture that in our proposed construction to indicate that you have the power source, the inductance and the regulating circuitry just as Figure 1 in the patent shows and just as they represented to the examiner over and over again that the claim should be treated as meaning and distinction of the prior art, but we know that from their position during this Markman proceeding they're going to argue the inductance coil can be downstream. It can't. That's exactly what they told

10:01 the examiner eight different times is different from their claimed invention. And so at the end of the day, Your Honor, we think the jury would be assisted by understanding what the claim language from, from a power source and an inductance means. They had to rewrite the claim to obtain confirmation of patentability during re-examination and they had to explain to the examiner eight different times that that meant the inductance coil could not be upstream.

Having said that, having made the amendment, we ask Your Honor that they be held to it.

THE COURT: Yes, ma'am.

MS. PROCTOR: Your Honor, can I make a brief response?

THE COURT: You have as much as time you want.

MS. PROCTOR: Thank you, Your Honor.

So a few points. Intel's counsel said at the beginning of his presentation 9:36 a.m. what really matters is what is claimed, and he actually said that a few times. We completely agree. That is what should control here what is claimed. And it is Intel who's trying to deviate from what is claimed, not VLSI.

He also said, at the end of the day, the claim language governs. Again, we could not agree more. That is really the answer here. The claim language is clear. The parties agree on that and it is what governs.

Now, you heard a lot from Intel's counsel about boost

converters and how those configurations fall within the scope of the claims. We agree, but here's how I like to think about it: So the -- let's say the claim covers something like the color purple, right? So the parties agree that lavender is a shade of purple. That doesn't mean that lavender -- that all shades of purple, that purple is now defined to mean lavender for all purposes, and that's what Intel's trying to do. They're trying to say, oh, well, everyone agrees boost can be one way to implement this. So let's limit everything to boost configuration. It's just not supported. And the fact that the patentee might have distinguished blue from purple doesn't change that. It doesn't then somehow support limiting the entire family of shades of purple to something like lavender.

Now, Intel distinguished buck configurations a few times based specifically on the inductor being downstream from the regulating circuitry. That's actually identical to the layout in the buck boost configuration.

If you can go to Slide 21, please.

So here we go. Power source on the left, battery, switch in the middle, inductor downstream. It is crystal clear from the re-examination history and from things like Claim 23 this configuration falls within the scope of Claim 1, period. And it is not a configuration where the inductor is -- it is a configuration where the inductor is downstream of the power source on the regulating circuitry, and that's precisely how

10:04 Intel tried to distinguish all buck converters.

10:04 You also heard a fair amount about how buck configurations operate, and Intel tried to distinguish what the inductor does in the buck circuit from what it does in a boost or a buck boost configuration. So Intel described for example the inductor as being smoothing here in a buck configuration. I don't necessarily disagree with that characterization, but it really is just that. It's a characterization. What's actually happening here is that when the switch is closed, some of that current is being stored in the inductor as magnetic field, and then when the switch is open, some of that stored energy is going to power the load.

10:05 If we look at buck boost, same thing. Switch is closed, power source is going to the inductor charging up the inductor. Switch is open, inductor -- that stored energy is going to power the load. It is really the same basic operation. Inductors are doing what inductors do, storing energy in a magnetic field and then providing that energy to the load. So this idea of smoothing is really not meaningful.

10:05 What it is meaningful too, though, is Intel's arguments about what from means. And I heard kind of a change in tone in Intel's argument today from -- in their brief they really are very clear the only support for these two limitations is the re-exam history. Today counsel tried to argue a little bit that somehow the plain and ordinary meaning of from supports

their construction. Well, if that were true, they would be relying on the patent itself to make those arguments, not the re-exam history for the re-exam history to be redefining terms were in the world of disclaimer, as they know and as they've tried to argue separately. So this really isn't a plain and -- what is the plain and ordinary meaning question.

Also even if it were, I don't agree. I think they're wrong on what from means here. So what we're regulating is the output voltage, right? And that output voltage is absolutely being regulated from an inductor and a power source and a buck or boost configuration. And you saw that actually in their own diagram. So they showed you how in the buck configuration if you don't have the inductor and take it away, you get that square wave, right, at the output at the load. Now, when you do have the inductor there, you get more of a smoothed out version. And so the output, the voltage that's going to the load, is absolutely being regulated from the inductance and the power source. Both of those components are what combine to provide that output voltage. And so it's not fair to say that somehow the plain and ordinary meaning of from limits us to Intel's boost only world.

They also talked a little bit about Claim 9 kind of in an attempt to make the same argument how Claim 9 was amended during the re-examination, and instead of being able to choose from a linear regulator, a power source and an inductance, it

had to be both the power source and an inductance. Absolutely. That's what Claim 1 has always said. Claim 1 was not amended, and all the arguments Intel relies on from the re-exam history are about Claim 1. So Claim 9 is really just an attempt to make it seem like there was some amendment that was relevant when really Claim 1 has always said from a power source and an inductance, and that's what was being discussed and was ultimately held to be valid.

So, Your Honor, at the end of the day here Intel says there's no mystery. But I also didn't hear Intel's counsel at any point show you where in the re-exam history it says the inductance has to be both connected to the power source and positioned between the power source and the regulating circuitry. It's not there. It never says it in the history. It is Intel's burden to show you with clear and unmistakable proof that the patentee limited the claim not just in some abstract way but limited the claim in the way Intel's arguing. So limited the claim to have -- the claims to have both those additional limitations. It's just not there. They have not met their burden, and plain and ordinary meaning should control.

Thank you, Your Honor.

MR. MUELLER: Briefly, Your Honor?

THE COURT: Yes.

MR. MUELLER: Just a few points, Your Honor. The first is

Ms. Proctor did not contest nor did VLSI contest in its briefing any of our explanations of how those circuits functioned in the eight prior art references. That is to say there's no dispute, no fact dispute between the parties that when we label something as having a power source and an inductance and a regulating circuit in particular positions, those are in fact where they're located. So this is not a situation where the parties have different views as to the underlying facts that were present before the Patent Office. Those eight prior art circuits, there's no dispute, function precisely the way that we've explained in our briefing to Your Honor. And in each and every one of those circuits there's a power source, a regulating circuit and then an inductance coil downstream, and in each and every one of those eight instances the applicants told the Patent Office that was different from what they were claiming. So, again, the issue here, Your Honor, is what does from a power source and an inductance mean? And they explain precisely what it means to the Patent Office over and over and over again.

If we could just go to one example, Your Honor, of the Dancy reference. This is Slide 8 of our Markman slides, Your Honor. And I showed you the slide earlier, but just to return to it briefly. Dancy's regulator down converter, however, does not regulate at least one supply from a power source at an inductance because the power supply control signal operates

switches S1 and S2 from the power source alone, not from the power source and the inductance as recited in Claim 1. They could not have been any clearer about what that means, Your Honor.

THE COURT: Is my understanding about the Dancy figure that it's just conceptual?

MR. MUELLER: I'm sorry, Your Honor?

THE COURT: Is my understanding that the Dancy figure is just conceptual and not an actual?

MR. MUELLER: It is, Your Honor, although it does show real world circuit components that could be configured in this way.

THE COURT: And is the Dancy example being used for voltage regulation?

MR. MUELLER: Yes. It is being used for conversion -- power conversion and the circuits that are claimed in this power conversion as well. So it's exactly the same field, and this is the -- exactly the same type of circuit we see in, for example, Figure 1 of the patent.

THE COURT: And what would one skilled in the art understand the word "positioned" to mean?

MR. MUELLER: Positioned?

THE COURT: Yes.

MR. MUELLER: Just located in the series where the current flows. You need to know in what sequence they occur and so

10:11 where it needs to be positioned in that sequence once the
10:11 circuit is closed and current begins to flow. That will
10:11 dictate the order of operations of the various circuit
10:11 elements.
10:11 And so here, Your Honor, where the regulating circuitry is
10:11 positioned in the Dancy reference and each of the other seven
10:11 is connected to the power source but before the inductor.
10:11 Again, no fact dispute on that. And this is exactly what they
10:12 said, does not regulate from a power source and an inductance
10:12 because -- because they use the word "because" -- it regulates
10:12 from the power source alone, not from the power source in the
10:12 inductance.
10:12 Now, Ms. Proctor just told you a few moments ago the
10:12 inductance could be somewhere downstream and there still could
10:12 be regulation from. That's not what they told the Patent
10:12 Office. What they told the Patent Office is -- because they
10:12 had that here. They had an inductor coil downstream, but they
10:12 told the Patent Office that's different, that when we say
10:12 regulate from a power source an inductance, what we mean is
10:12 regulate from both of them and that that's different than a
10:12 regulation from a power source alone, and they said it right
10:12 here. That's not from the power source in the inductance. So,
10:12 again, it's crystal clear on its face, Your Honor, under any
10:12 standard of review of the prosecution history. That is a
10:12 disclaimer. That is also a definition. That is whatever word

you want to attach to it. It is a statement about what the claim means and a position to which they need to be held.

And we thank you, Your Honor. Unless you have you any further questions.

THE COURT: I don't.

Do you have anything else you wanted to add?

MS. PROCTOR: Just very briefly, Your Honor.

I want to point out two things I did not hear Intel's counsel address. Number one is the buck boost converter that we spent a lot of time on and that the re-examination history makes extremely clear does fall within the scope of Claim 1, and that's demonstrated by, for example, Claim 23.

I also still have not seen an affirmative statement defining what it means to regulate from a power source and an inductance. I didn't hear it that time either. So at the end of the day Intel really is just guessing. They're make assumptions about what the patentee meant. They're interpreting figures, adding their own colors and boxes and then trying to guess, but that is just not good enough. You can't rewrite claims based on guesses.

Thank you, Your Honor.

MR. MUELLER: Your Honor, just one more brief thing.

THE COURT: You guys have as much time as you need.

MR. MUELLER: Okay. I appreciate it, Your Honor.

And Ms. Proctor did mention that I meant to mention, but I

forgot. The buck boost idea. So there are various ways that you can take circuit elements and add different things to them. So you could have in fact a boost with a buck conversion stage after it. And when I said at the very beginning of the day, Your Honor, that the label at the end of the day is not the most significant thing. What matters is the circuit elements as claimed, this is one example of that as well. If you had a circuit in which the regulating circuitry regulated from an inductance and a power source as claimed in the patent, you could have all sorts of things downstream. You could have a buck converter after that. You can add things to a claim -- to a claimed invention without escaping the scope of the claim. So we're not here to say that there's some negative limitation that precludes the addition of other circuit elements in addition to the ones that are claimed, and I couldn't even give you a full litany of all the different -- all types of circuit configurations that might meet this claim. What I can tell you, though, Your Honor, and what our position is is that they have to have this. They have to have regulating circuitry from a power source and an inductance. This buck boost converter that Ms. Proctor referred to was never once cited to the Patent Office in reference to those eight prior art references that we talked about earlier. What they said when they were discussing the prior art was what I showed you earlier. They need to be held to that, and that means that any circuit that would meet

this claim would have to have the regulating circuitry and the inductance in the power source upstream from that so that it can regulate from those two things. Beyond that, there's an infinite variation that could come downstream, additional components that could be added to it, but they have to have what they claimed. They have to have the claim requirements they relied on to distinguish the prior art. So the buck boost at the end of the day is a red herring, unless Ms. Proctor means to suggest that a buck boost circuit could meet the claim without an inductance before the regulating circuitry. It absolutely could not. There needs to be an inductance and a power source before the regulating circuitry so that it can meet the requirement from regulation from a power source and inductance. The requirement they relied on eight different times to obtain the re-exam claims, Your Honor.

Thank you.

MS. PROCTOR: And, Your Honor, I'm -- I just want to be crystal clear here because I think Intel's counsel attempted to address the buck boost circuit but actually talked about maybe a buck plus boost circuit. Very different. So going back to the buck boost converter we've talked about here, I just want to be clear. In this circuit the inductance is downstream of both the power source and the regulating circuitry, and this circuit in this way absolutely is within the scope of the Claim 1 and within the scope of Claim 23 even after the re-exam. So

they still haven't actually addressed the circuit that I've been talking about and focusing on.

Ultimately what he said at the outset is right. At the end of the day the claim language governs, and we agree. So Intel still has not shown any reason to rewrite the claims in a way that excludes Claim 23, excludes a buck boost converter and dramatically changes their scope.

Thank you, Your Honor.

MR. MUELLER: I'll just say we're not excluding Claim 23, and beyond that I've already made my arguments, Your Honor. Thank you.

MS. PROCTOR: Thank you, Your Honor.

THE COURT: I listen to a lot of Supreme Court arguments, and one of my have favorite things that Justice Pryor ever said was he told one counsel that I listen to what you say and I think you're absolutely right and then I listen to the other counsel and I think you're absolutely right. What am I to do? And I -- those were two very good arguments, and to those people who are taking their time to come and watch really great lawyers who are in the audience, you picked a great day to be here. All that being said -- and I mean it. Those arguments were exceptional. The Court is going to find that there was no clear and unequivocal disavowal. We rely in great part on what counsel has said with the allowance of Claim 23 and we find that it would allow both a boost and a buck converter;

10:18 therefore, the claim construction for the first term is going
10:18 to be plain and ordinary meaning.
10:18 Next claim up? I'm sorry. The next claim term up?
10:18 MS. WEN: Good morning, Your Honor. Charlotte Wen for the
10:19 plaintiff.
10:19 THE COURT: Good morning.
10:19 MS. WEN: So here to talk to you today about the '485
10:19 patent which is the patent that generally relates to the --
10:19 woops. Sorry -- concept of charge sharing. So as the patent
10:19 discloses --
10:19 THE COURT: Let me just go and make sure I'm on the same
10:19 claim term that you are. I think I am, but...
10:19 MS. WEN: Yeah. So there are a few claim terms for this
10:19 patent.
10:19 THE COURT: Okay. If you'll -- I've got a lot of papers
10:19 up here. If you'll let me know which claim term you're on and
10:19 I'll make sure that I'm on the right one in my stack.
10:19 MS. WEN: Sure. Capacitance structure is the first one.
10:19 THE COURT: Okay. I'm with you. Thank you, ma'am.
10:20 MS. WEN: Okay. So this patent generally relates to
10:20 memory cells. Memory cells, as you know, store memory, and a
10:20 memory cell that has high voltage is considered stable and can
10:20 hold the memory that it's supposed to be holding. Now,
10:20 however, if you wanted to rewrite the memory to that cell,
10:20 it -- a memory cell that is stable enough to hold voltage is

not capable of being written to very well. And so the '485 patent describes a charge sharing scheme that allows for charge to be shared between the memory cells and the capacitance structure during a write operation in order to make it easier for the memory cells to be written to.

So during this exemplary operation, the memory is decoupled from the power supply which allows it to be stable enough to hold memory and it couples to the capacitance structure to share a charge. And by doing this, the voltage in the memory cell is lowered which improves the writability, and so this a temporary lowering of voltage using a capacitance structure. And so capacitance is a physical characteristic. It describes a structure's ability to hold the charge. And types of structures that have capacitance include capacitors. They include transistors and they include, as disclosed by the '485 patent, dummy memory cells.

THE COURT: You'll make my court reporter very happy if you'll say -- when you're showing the slides which slide you're showing me.

MS. WEN: Sure. So we're on Slide 69 right now. And we're discussing the types of structures with capacitance.

And I just want to talk to you a little bit about the tutorial that Intel submitted. Intel's tutorial focuses a lot on two of the embodiments that are disclosed in the '485 patent, specifically in Figures 2 and 3. And we just want to

10:22 be clear that it is the claims and not the specification that
10:22 define the invention. Intel's tutorial confuses the
10:22 embodiments of the claims. It attempts to limit the claims to
10:22 Figures 2 and 3 and mischaracterizes the specification.
10:22 So as an example, Intel told you that this figure, Figure
10:22 2, is the invention of the patent. This is only an example
10:22 of -- this is only an example -- like an exemplary embodiment
10:22 of the patent. So, for example, the patent says that various
10:22 changes and modifications to the embodiments herein chosen for
10:22 purposes of illustration will readily occur to those skilled in
10:22 the art.
10:22 As another example, Intel's slide specifically says that
10:23 there is a plurality of dummy cells in the invention, but not
10:23 every single claim requires dummy cells. And, in fact, when
10:23 the patent introduces dummy cells, it says dummy SRAM cells are
10:23 coupled to the dummy bit lines and are conventional SRAM cells
10:23 in the illustrated embodiment only.
10:23 And so when you look at the claims, you can see that in
10:23 Claim 1 the patent claims a first capacitance structure which
10:23 includes a plurality of dummy cells. And in Claim 17, which is
10:23 a claim that we're going to be talking about today, the patent
10:23 does not claim a plurality of -- does not require the
10:23 capacitance structure to include a plurality of dummy cells.
10:23 Similarly, Slide 20 of Intel's tutorial pointed out that
10:23 there's a single dummy cell that is not coupled. And in

addition to what I was saying earlier that not every single embodiment requires dummy cells, not every single embodiment of a patent requires a single dummy cell that is not coupled. And so this is Slide 74 discussing Intel's tutorial at Slide 20.

And so I'm going to move into a discussion of the claim term which is a capacitance structure. And essentially the parties' dispute centers around the question of whether capacitance structure is a means plus function term or whether it should have its plain and ordinary meaning. As you know -- this is Slide 77 -- when a claim term does not use the word "means," there's a presumption that Section 112, Paragraph 6 does not apply. And the standard to determine whether the words of a claim are understood by persons of ordinary skill in the art have a -- is whether they have a sufficiently definite meaning as a name for structure. Now, Intel claims that the patent doesn't explain what a capacitance structure is, that it doesn't attribute any real -- it only discloses the location of the capacitance structure within the claimed memory circuit, but that's not quite right. A person of ordinary skill in the art would understand that the capacitance structure refers to a specific class of structures. So, for example, as Slide 79 shows, the '485 patent provides multiple structural examples, and I'll go through several of them of what can comprise a capacitance structure.

THE COURT: Is it -- is it your position that the term

"capacitance structure" is well-known in the art as a structure?

MS. WEN: I think it's our position that a person of ordinary skill in the art would understand the term "capacitance structure" particularly within --

THE COURT: To be a structure?

MS. WEN: To refer to a class of structures.

THE COURT: Okay. So -- and I did what I do which is my skill set as a technology person which is I Googled it and -- which is -- obviously I'm not one skilled in the art, but we came up with about 4,000 hits when you Google capacitance structure, and that's why I'm forecasting for Intel what I'm going to be curious to hear from them as to why it's not thought of regardless of what's in the patent or, rather, in addition to what's in the patent that it wasn't already a well-known term and a set of structures.

And also, and I've said this before, but I think it's worthy of repeating because it's -- my philosophy is, you know, I never had to -- or would be allowed to write a patent, but I am sympathetic with those who do, and when someone is writing a patent like this and they use a term like "capacitance structure" and they are, my guess is, presuming that people will know what it means, I think it's fair to not upset that process and make the people drafting patents feel like they have to explain everything as well or be its own risk. So

10:27 that's just my -- I may be right or I may be wrong, but that is
10:27 my general philosophy on how I interpret when a -- when a term
10:27 like "capacitance structure" is challenged, it is a relatively
10:27 heavy burden on the people who are challenging it to persuade
10:27 me that I should disturb what the scribner did if he was in
10:28 good faith in thinking that it would be understood by a person
10:28 skilled in the art.
10:28 MS. WEN: So yeah. I agree with that completely, Your
10:28 Honor. I think a person of ordinary skill in the art upon
10:28 reading the '485 patent would understand that the capacitance
10:28 structure term refers to a broad class of structures. And so
10:28 I'll just go through these quickly. It explains how a
10:28 capacitance structure interacts with other structures on the
10:28 claimed memory circuit, and to provide even more color to what
10:28 the capacitance structure means, it describes the role of the
10:28 capacitance structure plays in the charge sharing scheme
10:28 described in the '485 patent.
10:28 So this next slide, Slide 80, just provides a long list of
10:28 examples of the various structures disclosed in the '485 patent
10:28 that can correspond to the capacitance structure. And so we
10:28 have memory cells. The patent says, for example, that in
10:28 another embodiment the supply voltage is reduced during the
10:29 write operation by charge sharing with a dummy column of memory
10:29 cells. The patent disclosed, as another example, dummy rows
10:29 and dummy columns. I'm not going to read out the entire slide,

but as another example, the patent explains that the relative capacitance between the dummy column and the memory array columns remains substantially constant for any number of rows. So this goes back to what I was talking about earlier where the memory cells that are being written to share charge with a capacitance structure. And in this particular embodiment the patent is talking about a dummy column.

Also disclosed by the patent are dummy cells and dummy SRAM cells, and the patent is careful to explain that while it is discussing conventional transistor SRAM cells and other embodiments, the type of a cell may be different.

So as I was saying, Intel has cited a case that -- from the Federal Circuit that found a claim term check standby unit to not recite structure because it did not include any examples of what structures or class of structures could fall within the definition. And here the written description does include a whole litany of examples in Slide 80.

In addition to providing multiple examples of the capacitance structure, the patent attributes specific structures within the claims to the capacitance structure. So you can see in the next few slides, beginning with Slide 82, that the patent contemplates several different types of configurations of capacitance structures. And, for example, Claim 3 requires a dummy line and a plurality of dummy cells coupled to the dummy line. Similarly, Claim 19 requires the

dummy line and also a first dummy cell adjacent to but not coupled to the dummy line.

And of course, if I go here, there are multiple claims in the patent that include additional structural limitations.

Similarly, during prosecution, the prosecution history's not very long, but the examiner noted that one of the claims of the '485 patent should include a plurality of dummy cells as a descriptor for a capacitance structure. So that indicates to me that the examiner also understood the capacitance structure recites structure.

It goes back to this slide -- Slide 86 goes back to Intel's argument. The Federal Circuit has noted that when dependent claims add limitations that describe particular structural features, that indicates that the patent has structure or the claim term recites structure, rather.

Third point, the patent also explains how the capacitance structure interacts with other structures in the circuit. It is coupled to various structures, including the power supply line in Slide 87 and in Claim 1. In Claim 6 there's a switching transistor coupled between the capacitance structure and a voltage reference terminal. And these are just further examples of the idea that the inventors clearly contemplated that the capacitance structure is a structure.

So the Federal Circuit when deciding whether a term is or is not a means plus function considers whether a person of

10:32 ordinary skill in the art would ascribe function to a particular claim term. And it is clear that capacitance structure does not recite a function.

As VLSI has explained -- as our expert Dr. Conte has explained, capacitance is a physical characteristic that describes a structure's ability to hold charge, and this is supported both by Dr. Conte by the patent and as well as one of the dictionary definitions that Intel provided.

So could we have DX28? That's Intel's Exhibit 28. I also have the paper version.

Okay. So if you see the definition of -- the definition of capacitance is what Intel cites in its briefing, and we think it also supports our construction, but if you look at the definition of capacitor, this definition here which says a component which has capacitance makes clear that a person of ordinary skill in the art would not understand capacitance to be a function. It is a physical property that components have.

Okay. Sorry for that. Could we go back to the slides?

So further supporting the fact that the capacitance structure does not recite a function. The phrase "providing capacitance" does not appear anywhere in the intrinsic record. Intel hasn't cited any particular part of the record that states that phrase, and the claims never ascribe any function to the capacitance structure. Only structure. As I showed you in many previous slides, all of the claim terms that include

capacitance structure only describe it in terms of structure.

And consistent with that definition that Intel provided, the '485 patent repeatedly describes structures as having capacitance. For example, it states that the capacitance of dummy Column 17 can be adjusted. The capacitance of dummy Column 17 is reduced and a relative capacitance between the dummy column and the memory array columns remains substantially constant. So the patent repeatedly refers to capacitance as a property that the structures have.

And so as VLSI has explained in its briefing, a person of ordinary skill in the art would understand capacitance structure by its plain and ordinary meaning as a class of structures with capacitance that can be used in the charge sharing scheme claimed in the '485 patent.

And just as a note, the Federal Circuit has held that it is sufficient if the claim term is used in common parlance or by persons of skill in the pertinent art to designate structure even if the term covers a broad class of structures.

And that is all from me.

THE COURT: Thank you.

Mr. Lee, good morning.

MR. LEE: Good morning, Your Honor.

Your Honor, we're handing out copies of both the Markman slides and the tutorial slides. May I proceed, Your Honor?

THE COURT: Absolutely. Yes, sir.

10:37 MR. LEE: While I have the podium, let me say three things. First, Mr. Yi e-mailed earlier today about the precharging means limitation, and I should report at least for Intel we are fine with the proposed construction of the Court.

THE COURT: Okay.

MR. LEE: Let me do two things while I have the podium now. One is to provide a little bit of bait to our tutorial which Your Honor has said and then to move to the capacitance structure, and while I understand Your Honor has articulated the hill we have to climb and hopefully we'll be able to present you with an argument that will at least cause you, in Justice Pryor's words, to pause on what the correct claim construction is.

So if I turn to the tutorial first, the one thing I would mention is the priority date is 2006, and I think that becomes important when we come back to what happens when you, for instance, would research or Google the term "capacitance structure" as of the priority date. If I turn --

THE COURT: That's a good point.

MR. LEE: Sure.

THE COURT: I don't know that we were that -- I don't know that we were that careful at looking and seeing what would -- which of those were from the appropriate date.

MR. LEE: Yeah. Your Honor, I think the key thing here for this record, and I'm now mixing the Markman hearing with

10:38 the tutorial, is this: You have multiple declarations from Dr. Conte. In terms of providing you with a publication, a peer reviewed journal, a dictionary as of the relevant time or close to the relevant time before or after that said capacitance structure as opposed to capacitor has an accepted meaning which was Your Honor's question, there's nothing.

THE COURT: Yes, sir.

MR. LEE: I mean, they had that opportunity to present it to you. There was nothing.

Your Honor, I wouldn't disagree that the word "capacitor" has an accepted meaning among engineers, but Your Honor will read this patent forever and you'll not find the word "capacitor."

THE COURT: Right.

MR. LEE: There's only capacitance structure, and I think that becomes important because, as Your Honor said, you know, it's hard to second guess the patent drafter, but the other fact is the patent drafter has a pen in his or her hand.

THE COURT: Well, no. And you are, by the way, very -- not surprisingly, given your great reputation, you are immediately hitting on a number of the things my law clerk and I were specifically discussing issues that we talked about in preparing for this -- the difference between capacitor and capacitance structure, and those -- these are -- you're touching on a number of things that I think are important and

10:40 that we have been discussing trying to get this right.

MR. LEE: And, you know, I will try, Your Honor, when I get into the substance of capacitance structure to try to address those specifically, and with Your Honor's indulgence I may take two or three minutes just to go --

THE COURT: You have all the time.

MR. LEE: So just for tutorial purposes, and I don't think there's any real disagreement about this, the patent is talking about static random access memory or SRAM. It is, if we go to Slide 3, a conventional form of computer memory. It is static, Your Honor, because unlike other certain types of memory, the data doesn't have to be periodically refreshed. It is random access, and this is important because any address, any of these cells can be written to or read from randomly.

If I go to Slide 4, Your Honor, the SRAM memory is typically structured as an array of memory cells, each holding one bit of data. They're typically in these lines rather than rows or columns. That becomes important for this patent because Figure 2 has the cells in columns. Figure 3 has them in rows, but it is fundamentally the same type of structure.

If I move to Slide 5, in order to store data in an SRAM cell, a voltage supply has to be applied to the cell, and that's what's shown in Slide 5. So each cell in the array has to be connected to a power supply, and the way you connect it is through a line.

10:41 Now, if I go to Slide 6, Your Honor, there's a tension in
10:41 setting voltage for SRAM memory cells, and the tension is what
10:41 leads to the claimed problem that the patent addresses. A
10:42 higher voltage provides better stability for the cell. On the
10:42 other hand, the lower voltage makes it easier to write to the
10:42 cells. So depending on what you're doing, you may want to have
10:42 a higher voltage or a lower voltage.
10:42 Well, before the filing date of this patent, if I move to
10:42 Slide No. 7, and I don't believe there's any disagreement about
10:42 this, this tension was resolved by having voltage high during
10:42 normal operations but lower during the write operation. It's
10:42 very logically called write assist by those of skill in the
10:42 art. There were other ways to do write assist which are
10:42 disclosed in the file history. The specific type of write
10:42 assist that's described in this patent is shown at Slide 8 and
10:42 it involves charge sharing. And specifically it describes a
10:42 circuit that uses charge sharing with dummy cells that during
10:43 the course of the write operation to a set to a row or a line
10:43 of cells.
10:43 Now, on Slide 9 we just briefly address the issue of
10:43 capacitance. Again, I don't think there's any disagreement.
10:43 Capacitance is the ability to store electrical charge. One
10:43 important point that wasn't mentioned by VLSI, but, again, I
10:43 don't think there's any real disagreement on, is this. Almost
10:43 every component, including conductors, have some capacitance.

They may not be intended to be a capacitor, but they will have some capacitance sometimes when it's unintentional and unwanted it's called, Your Honor, parasitic capacitance, but every component and conductor will have some capacitance, and that becomes important as we move through some of these terms and the means plus function arguments that we have to make to Your Honor.

THE COURT: Well, and what you might keep in mind as you are making that argument too, which is another issue that my clerk and I spent some time talking about, is this exact one is if I determine that plain and ordinary meaning applies or that it is not a means plus function, what would that do to the validity -- what would that -- how much would that expand Intel's ability to find prior art if every component could actually be a capacitance structure? You know, what impact would that have on it or -- and I guess on the infringement side as well, but I get that the plaintiff is saying, look. We gave you examples in a Jui Jitsu move, almost, which you are doing, if every component is a capacitance structure, what does that do to the validity of the patent?

MR. LEE: Your Honor, it for sure would have consequences. It would -- as Your Honor I think suggests, it would expand the scope of the prior art that might fall within the scope of the patent. It also would create real definiteness problems because how much is -- how much is enough and what is enough to

be enough. And if every component has an electrical capacity of some degree, how much is enough? Now, there are other limitations in the claim to be sure, but there would be some substantial validity implications.

THE COURT: I just am throwing that out there because it's something my clerk and I have already -- have already been thinking about. If we go with the plaintiff's construction, the impact it would have on that claim as well.

MR. LEE: And, Your Honor, that's in part -- when I get to capacitance structure, that's in part the reason we can -- we think we can make the Section 112, Paragraph 6 argument a principal argument, Your Honor, because it is something that would allow the patent to have some meaning, the term to have some meaning.

THE COURT: You would be doing it to help them out.

MR. LEE: Yeah. Not quite yet at least.

THE COURT: Okay.

(Laughter.)

MR. LEE: If I go to Slide No. 10, Your Honor, because virtually all components in an integrated circuit can store a charge, the voltage of one circuit can be lowered by connecting that circuit to another circuit.

Now, in the animation that we have now and on Slide No. 10 -- if I move to Slide No. 11, I have two circuits. And when the circuits are isolated and there is a voltage coming --

charge coming from the left-hand side into Circuit 1 but there's no connection to Circuit 2 because they're isolated, there will be no charge sharing. It's just sort of a logical demonstration of what charge sharing would be.

But if I move to Slide 12, if the circuits are coupled to each other, charge from Circuit 1 can be shared with Circuit 2, and the consequence of that sharing is to -- if I move to slide -- the last version of Slide 12 -- is to equalize the voltage between the two. It reduces the voltage in Circuit 1, increases in Circuit 2. And that's sort of the premise of the charge sharing that's described in the patent.

The '485 patent describes this specifically. And if I move to Slide No. 13 which is Figure 2 -- and, Your Honor, the figures are important for two reasons. One is claim language determines the scope of the claim, but they're to be read in light of the specification, and this specification is very specific.

The second is there's no dispute that the other four limitations before Your Honor are Section 112, Paragraph 6 limitations. They are by definition limited to the structures disclosed. So this patent is one where the structure -- the specifications disclosure is critically important. So the Figure 2 shows charge sharing principle. It does it with columns. If I click, there's a first line of memory cells in green on Slide 13.

10:48 THE COURT: And that would be on the left?
10:48 MR. LEE: Yes.
10:48 THE COURT: Yes, sir.
10:48 MR. LEE: A set in blue in the middle labeled Second Line of Memory Cells. And then on the right are the dummy cells. They are also, Your Honor, conventional SRAM cells. That's what the patent discloses.
10:48 If I move to Slide 14, the patent discloses also a power supply terminal, and that's the word that it uses. I don't think anybody disagrees that that has a meaning and it is a thing. And the power supply terminal is what provides the voltage to the memory cell.
10:48 THE COURT: Is there any disagreement between the parties how big the purple square on Slide 14 should be -- how much that -- the componentry, for example, that it does not include 52 and 50?
10:49 MR. LEE: I don't think that there's any dispute that the -- what's in purple is a power supply terminal. I think there are disputes as you move to the components between the purple box and --
10:49 THE COURT: That was my question.
10:49 MR. LEE: And that comes to some of the other terms that are before Your Honor.
10:49 THE COURT: Okay.
10:49 MR. LEE: And what happens, Your Honor, if we have in mind

10:49 that the idea here is that you're trying to write to one set of
10:49 cells but not to another so what you want to do is keep the
10:49 voltage highest to the one you're not writing to, allow them to
10:49 go lower to the set of cells that you are writing to, and the
10:49 way you do that is for that set of cells, you share the charge
10:49 with the dummy cells and you just pull some of it off. As
10:49 Slide No. 15 shows, each line of the memory cells has its own
10:50 power supply. It carries charge to the memory cells.
10:50 And as Slide 16 shows, I've now just focused on the second
10:50 line of memory cells which is the set of memory cells in this
10:50 example that we're writing to. So it's the one that if you're
10:50 writing to this set of memory cells, Your Honor, this is the
10:50 one where you're going to bring the charging to. If you
10:50 flipped it and you're writing to this one and you wanted not to
10:50 write to this one, you would just flip the exercise, but it
10:50 would be the same analytically. So if Column -- if the blue is
10:50 the second set of cells, here's what happens in Figure 2.
10:50 If you go to Slide 17, for the first set of cells that
10:50 you're not writing to that you want to maintain the voltage of,
10:50 they're connected by this first power line. That first power
10:50 line as shown in Figure 2 is not connected to the second line
10:51 of memory cells. It never is connected to the second line of
10:51 memory cells.
10:51 Instead, if we go to Slide No. 18 where we've now put in
10:51 red the dummy cells on the right, the second line of memory

cells in blue in the middle, the second line of memory cells will have its own power line.

THE COURT: Right.

MR. LEE: Now, what happens when you want to write is this: You decouple that second line to the power supply voltage, and at that point in time the transistor will couple the second line of memory cells to put out plurality of dummy cells and that will then pull the charge off, and the consequence of that, if I move to Slide No. 19, is to reduce the voltage in the second line of memory cells, increase it in the line of -- in the dummy cells and allow you to write assist.

And as the patent says, if I move to the last slide of the tutorial, you can affect the amount of charge sharing by selecting the number of dummy cells that you want to count. So an example that I'll use now on the very last slide is if I were to decide not to use 30 and just use 32 and 34 on the right-hand side, you would reduce the charge sharing.

So, Your Honor, let me move to capacitance structure if I could.

THE COURT: Yes, sir.

MR. LEE: And I will try to address the issues Your Honor raised during VLSI 's argument but also make our affirmative argument.

In the Markman slide -- so let's start at Slide 4. And,

10:53 Your Honor, I know you're very familiar with the Section 112, Paragraph 6 claim limitations. I do this in part because whenever I come to one of them, it's useful to remind ourself where they came from and what the problem was they were trying to address. And I think that will become important in answering Your Honor's question about capacitance structure even though it doesn't have the word "means" in it.

And Section 112, Paragraph 6 comes from a case decided almost 150 years ago, and it was the Morse case where he invented the telegram.

THE COURT: Sure.

MR. LEE: And he had eight claims. Seven were apparatus claims, but the last claim was, I'm claiming anything, right? Anything that will perform the function of electronically transmitting information.

THE COURT: I'm claiming electricity.

MR. LEE: Basically it. And, you know, if the patent had had a 100 year term, it would have covered the internet, covered anything, and the Supreme Court said, no. You can't do that. We're not going to have functional claiming because it would -- you know, if you allow people to claim functionally, it would just basically carve out huge portions and preclude innovation in the area.

So if I go to Slide 5, Section 112, Paragraph 6 is the answer. And I'm actually going to -- on this slide go from the

bottom -- start at the bottom. And this is the point that I think is important as we look at capacitance structure and actually as we look at the disclosed structure for the other limitations in dispute.

The point of Section 112, Paragraph 6 is to, and I quote, "avoid pure functional claiming." That's the purpose. So what you have to do, you can have a functional claim, but then you're limited to the disclosed structure and structure equivalence, which I know Your Honor knows. I think it's important that we all just keep in mind that the purpose of that is to avoid functional claiming. And if the end result of interpreting a limitation would be to allow functional claiming, then that's what Section 112, Paragraph 6 is intended not so much to preclude, Your Honor, but to limit, and limit you to the structure you've disclosed.

So if I move to Slide No. 6, the result of that is the two requirements identifying the claim function and then determining what the structure is in the spec that is clearly linked to the function of the claim.

So with that in mind -- and I'll come back to the law only briefly to discuss the Williamson case when we get -- as part of the argument on capacitance structure, but let me turn to capacitance structure. Well, and if I move to Slide No. 8, we have the competing claim constructions.

Now, Your Honor, I think literally if it were a means plus

function limitation, what we've described is a disclosed structure. I think if Your Honor concluded for any of these that it is a means plus function, this is what the specification disclosed, you might tell us to meet and confer to see if we could save the structure on a simpler basis, and I think that we could, but we haven't done that yet but we could. VLSI is plain and ordinary meaning. And, again, having had multiple chances now to say the capacitance structure is a well recognized term in the field, there's nothing that the expert relies upon to say -- in fact, Dr. Apsel, our expert, says it's not. There are terms that are well recognized and I'll come to those.

So the real question, if I move to Slide 9, is, is it a Section 112, Paragraph 6 limitation?

And let me take Your Honor to Slide 10, because I think this is -- the Williamson case is important. Whatever presumption there might have been before Williamson is certainly different today, and the key part of Williamson is it said, look. If you don't use words like "means," but you use words like "mechanism," "element," "device" or other nonce words, they're not disclosing sufficient structure. Stated differently, Your Honor, you're functionally claiming. Why is this important now? Because if we look at the way that it was articulated by Williamson -- and this is the second bullet point on Slide No. 10 -- what they say is these words like

10:58 "mechanism," "element," "device" reflect nothing more than
10:58 verbal constructs. It is tantamount to using the word "means"
10:58 because they typically do not connote sufficiently definite
10:58 structure.
10:58 So what they're saying is these words "mechanism,"
10:58 "element," "device" or other words like it are insufficient
10:58 because they're not defining structure. These are all words
10:58 that are just under the umbrella. They're subsets of a word
10:58 structure. If they aren't disclosing sufficient structure,
10:58 then the broader term "structure" is not. And at Pages 11 and
10:58 12 of our briefs, Your Honor, there are cases that have dealt
10:58 with claim terms like "attachment structure" and said, no. No.
10:58 No. That's a nonce term. It's Section 112, Paragraph 6.
10:59 Now, if I turn you to Slide 11, capacitance does refer to
10:59 a function. A capacitor, as we said earlier, would refer to a
10:59 thing, and there is no dispute between -- there's certainly no
10:59 dispute from us that capacitor has a recognized meaning to one
10:59 of ordinary skill in the art, but as I said earlier, you won't
10:59 find that word in the patent.
10:59 And, Your Honor, if I took you to VLSI's reply brief at
10:59 Page 4, they actually list specifically what was disclosed in
10:59 the patent to perform this charge sharing function, this
10:59 capacitance structure. The word "capacitor" is not there in
10:59 any respect. In fact --
10:59 I don't know. Can you bring up their slide? No? Okay.

10:59 Can we flip to the ELMO?

11:00 All right. So, Your Honor, I'm going to put on the screen their Slide 30. And, Your Honor, this is a slide they just presented to you now on what is disclosed.

11:00 THE COURT: Yes, sir.

11:00 MR. LEE: And there -- this is actually largely correct. It does disclose memory cells, but, as I said, these dummy cells are just memory cells. They are cells but not used for memory purposes.

11:00 Then look at the categories, Your Honor. Dummy rows, dummy columns, dummy cells, dummy SRAM cells. That's it. Not transistors, not capacitor, not any other well recognized term and no suggestion that there is a well accepted meaning, and that's because if we go back to Slide No. 11, capacitance refers to a function, and actually both experts agree, and we've quoted from both declarations. It refers to the ability to hold an electrical charge. It refers to the ability to store a charge. It refers to a function.

11:01 As a consequence, if we go to Slide No. 12, our expert Dr. Apsel opined the capacitance structure, that term itself, doesn't have any plain and ordinary meaning to when a -- recognized meaning to one of ordinary skill in the art because, and this goes to Your Honor's question, virtually every component has some capacitance.

11:01 Now, probably the best answer to Your Honor's question

about capacitance structure and whether it has a well recognized meaning is actually Dr. Conte's declarations offered by VLSI and I have them on Slide No. 13. He says that capacitance structures are a well-known class of structures such as those on a memory circuit that have capacitance. Well, that is just describing it by the function.

And then he says, such structures can include, for example, transistors, capacitors, dummy cells and arrangements of the same which have capacitance.

He then doesn't cite for Your Honor any journal, any dictionary, any publication, contemporaneously or not, that would demonstrate this.

And, in fact, by the time he gets to his second declaration, his definition gets a little bit more precise. It's actually 100 percent consistent with this being a Section 112, Paragraph 6 claim. A class of structures with capacitance. So it's just a structure, right, with the ability to store described in the '485 patent. So he's saying, here's what it is. It is something that can perform the function of storing charge as described in the '485 patent, that is, the dummy cells, and that actually is what we have asked the Court to identify as the structure. If there is -- if this were a Section 112, Paragraph 6 claim as a matter of law, there's no dispute about what the structure is. It is these dummy cells.

So, Your Honor, it's -- if I go to Slide 14, there's no

dispute that the disclosed capacitance structure in the embodiments in Figure 2 and 3 are the dummy cells. This is shown in Figure 14 on the right in the red block and Figure 15 -- I'm sorry. Slide 15 in Figure 3 in the red block.

So let me come to Slide 16, and an argument that was made to you this morning, which I think is legally not quite right, and that is because of other claims, it has to be that the capacitance structure must be broader than dummy cells. The first argument is that claims that say a first capacitance structure includes the plurality of dummy cells, if you took our reading, you would be limiting the claim to that. That's not true. And, in fact, Your Honor, the IMS case from the Federal Circuit says that's not right.

This on the left, Claims 1 and 12, would not include structural equivalence, dummy cells. So you would -- it could be dummy cells, but without the plurality of dummy cells, it would be dummy cells for structural equivalence. This is narrower.

And Claims 3 and 19 both have additional limitations as shown on Slide No. 16 and those additional limitations all add more.

If I go to Slide 17, let me answer a couple of the questions Your Honor posed to suggest the hill that we had to climb. And I think that there are a number of different answers. The first is, as I said earlier, what's relevant is

what was known to one of ordinary skill in the art at the time of the filing and, two, what was publicly available in terms of dictionaries, publications, and the answer on that is there's nothing in the record that VLSI has suggested provides that definition.

The slide that VLSI offered you has the disclosed structure. They're all dummy cells. And when Dr. Conte went to -- when Dr. Conte went to describe what this class of structure was, he defined it by function or what's in the '485 patent. That's all that we're asking.

Slide 17 I think has the answer to the question Your Honor asked in anticipation, which is, if it's just plain meaning and anything with any structure, anything with capacitance would satisfy that limitation, it's indefinite, and we would be back to you not quite apart from the prior art question and how big a door you open up. We would be back to you. So, Your Honor, we recognize that, as I said to our folks, we sat down, as you sat down to look at the claim, the claim term capacitance structure doesn't use the word "means" like the next four paragraphs do. What do you take from that? Well, one thing you could take from that is they didn't intend for it to be Section 112, Paragraph 6 which I think may be implicit in Your Honor's question.

The other thing you could take from it is this: They had a very specific method of write assist, and what they were

doing in their specific method was taking something that was basically functional in its articulation description and claiming it in a specific way that allowed them to get a patent.

The capacitance structure limitation has any disclosed structure. It is only the dummy cells that they gave you on their own sheet of paper. It had -- on this record it had no plain and ordinary meaning. Dr. Conte doesn't suggest otherwise. It had no support in dictionaries, publications or peer reviewed journals. It had only the disclosure of the dummy cells. So the question is, is an interpretation that would walk right into an indefiniteness problem because everything has some capacitance the correct interpretation, or is the correct interpretation one that says, no. There's not enough structure here to disclose. No. It doesn't have a recognized meaning. The correct interpretation is something that provides capacitance. What's disclosed in the patent? Both in Figures 2 and Figure 3, which are a part of the patent, it's the dummy cells.

THE COURT: Yes.

MR. LEE: Thank you, Your Honor.

THE COURT: No. Thank you.

Let me tell you my discussion with Mr. Lee was confusing. I mean -- I don't mean that in a bad way. I mean, it makes it tougher for me to decide what to do. I am concerned -- I am

probably of the opinion -- I'm reluctant to find that this is a 112. I'm reluctant to go with what Intel has proposed; however, I'm reluctant to say plain and ordinary meaning for the reasons that we stated, and I am very sympathetic with Mr. Lee's position that it ought to be dummy -- that even plain and ordinary meaning ought to restrict the claim to dummy cells in some manner. So help me out on what I should do.

MS. WEN: Sure. I think that the disclosure is broader than just dummy cells. I think dummy cells like we showed you in the slide previously are examples of capacitance structures provided by the claims.

THE COURT: I'm -- I certainly get the argument that you aren't going to be restricted by what was -- you know, I get that argument. I'm trying to be more helpful to you and to Intel. I'm trying to be more helpful saying that if we don't -- in a situation where every component might be considered to be a capacitance structure not tethering it to any group of any particular cells seems to me to be very problematic for VLSI. And so I'm trying to -- lifeline is probably the wrong way of phrasing it, but I do need you to help me figure out what to do in lieu if I were not to go with -- generally speaking with what Mr. Lee has suggested for Intel and then allowing you all to say what the appropriate structure ought to be through some meet and confer. At a minimum I need you to help me with what would be meant by plain

and ordinary meaning with respect to what a capacitance structure is. If you can't do that, then I think I'm just setting everyone up for me to have to face an indefinite argument.

MS. WEN: So I think we would be okay with a construction that is, for example, a structure that is used to provide capacitance, and we think that the -- so Intel was saying that the disclosure of the capacitance structure could include virtually any component on an electrical circuit, but I don't think that's true. As we explained -- let me see if I can go back to the right --

THE COURT: And I get the other -- that the other claim elements help you out.

MS. WEN: Yeah.

THE COURT: Because to take away from Mr. Lee's concern in line that any component could be a capacitance structure, they -- there will be no argument that they might meet the terms of the patent because they wouldn't have the -- they wouldn't have the other elements, but I'm still -- but I do want to get this right. Even if I give a plain and ordinary meaning, I want to make sure that you all don't leave here having different opinions of what the plain and ordinary meaning is. And then if I do that and Intel thinks that the appropriate thing to do is to then file some kind of motion with regard to indefiniteness, I'll take it up at that point.

MS. WEN: Okay.

THE COURT: But if we -- but I'm looking for your help in terms of what I should say plain and ordinary meaning is with regard to what a capacitance structure is to make sure at least you all know what -- at least so it's clear what plain and ordinary meaning is.

MS. WEN: Okay. So, like I said, we would be fine with a structure that is used to provide capacitance, and we think that it is far more limited than what Intel was saying. As I explained earlier today, the '485 patent discloses a scheme for charge sharing, and as part of the scheme, there are lines of memory cells that are selected for writing. And the charge sharing essentially enables that writing. So when you select a line of memory cells for writing, you couple it to the capacitance structure so that it can share a charge with that structure. And so the capacitance structure is necessarily limited to a class of structures that is actually capable -- it has enough capacitance to enable this charge sharing. It's not completely arbitrary. It wouldn't just include a conductor, for example. It would include a specific class of structures like Dr. Conte explained like we've been explaining, and --

THE COURT: So, and I may be wrong, but there's a difference in my mind between the language a structure that is used to provide capacitance versus me saying plain and ordinary meaning would be a structure that is capable because it may or

may not be being used to provide capacitance. I've worked hard on trying to say this right. I'm not doing well. "Capacitance." Is your -- would your proposal be that it is a structure that is capable of providing capacitance or a structure that is used to provide capacitance?

MS. WEN: I think we would want a structure that is used to provide capacitance.

THE COURT: Okay. And you think that would limit the universe of what components -- sufficiently limit the components in the products in a manner that would make a capacitance structure not indefinite?

MS. WEN: Yes. We think so, especially in the context of the '485 patent because it's important to note that these claim terms don't exist in the abstract. They exist in the context of the claims and the specification.

THE COURT: I get that. Did you have anything else you wanted to add?

MS. WEN: No.

THE COURT: Okay. Thank you, ma'am.

Mr. Lee?

MS. WEN: Is that all you wanted?

THE COURT: Unless you -- if you had more, I didn't mean to cut you off at all.

MS. WEN: Oh, I just -- I wanted to go back to --

THE COURT: I want you to do whatever you -- that's all I

had on that point, but you're welcome to finish any argument you had.

MS. WEN: I'll step down for now.

THE COURT: Okay. Mr. Lee?

The bid on the table is either what you would like, which I understand why you want. You don't need to repeat that. I get why you think it should be that. Versus plain and ordinary meaning which the Court would understand that the structure had to be used to provide capacitance.

MR. LEE: Your Honor, I think it would still have the same problem that you're not -- I want to set aside the heart of the argument --

THE COURT: Yes, sir.

MR. LEE: -- I tried to climb up hill on. So I set aside the 112, Paragraph 6 arguments and focus on a different interpretation that would be plain and ordinary meaning and an articulation of that.

The problem that we would have, respectfully, with that articulation is a structure that is used to provide capacitance is just defining it by function. I actually think it's almost even more problematic because it is taking the function to provide capacitance and then somehow there's a question of what you intend it to be. You know, if you intend it to be --

THE COURT: I get that.

MR. LEE: And I understand that that might deal with the

fact that there are these unwanted capacitance that's out there, but I don't think that would solve --

THE COURT: And it does sort of a little bit back to the Supreme Court case where he was saying if I use it to do that, then I'm -- then it's covered.

MR. LEE: Right. Right. Yeah. That's -- that would actually be functional claiming. That's actually --

THE COURT: That would actually be a function -- yes. I get that.

MR. LEE: It would be the eighth claim of Morse's effort to claim everything.

I think that if there was going to be -- if you took a person of ordinary skill in the art reading the patent, knowing what a capacitor was, knowing what a transistor was, knowing what an inductor was, and they read this patent and saw there were a capacitance structure, what they would understand the capacitance structure to be is dummy cells because that's what it said in words. And if you recall the slide I put on the screen from their presentation to you today, it's only dummy cells.

THE COURT: Yes.

MR. LEE: So I think, Your Honor, if we sort of took a Phillips look at it, which is, how would one of ordinary skill in the art look at this patent and specification? How would they look at Figure 2 and 3 when capacitance structure on this

record has no demonstrated accepted meaning. There's no definition in the patent itself. They don't ever call the capacitance structure suggested in Figure 2 or 3. It's transistors or capacitors. And instead what they do is specifically say dummy cells, and the dummy cells are specific to the claim because that is what is different from the prior art, and so I think if it was going to be a plain and ordinary meaning, it would be plain and ordinary meaning which is dummy cells.

THE COURT: Got it.

Counsel, anything else for VLSI?

Actually, let me tell you what I'm going to do just to save us time. I think I've -- and I hate doing this because I like having you all leave with these things resolved in a way I set things up, but what I'm going to do is have you guys get me a formal proposal of what you want plain and ordinary meaning to be. Meet and confer first. If you can't work it out, you can't work it out. I get that. I certainly understand and am probably -- at the moment leaning towards something that identifies it as dummy cells unless I can be persuaded why it ought to be broader, and -- but I'm going to have -- I'm going to give you guys an opportunity to meet and confer, and let me know by Monday or Tuesday what your proposal is. And unless you have something you want to add right now, I'll rule -- we'll either pick between what is proposed or do something and

11:20 you'll have it very quickly next week, but I want to give you all a chance to make this more formal than just winging it here and trying to get it right. So does that -- is that agreeable to everyone?

MR. LEE: It is for Intel. Could we have till Tuesday, Your Honor, just because people travel?

THE COURT: How about till Thursday? I want to get it to you -- I'm not trying to -- I'm trying to get it done as quickly as possible for you all. So if you'll have it to us by Thursday of next week. It's not going to take us a long time to make our minds up. You'll have the decision next week.

MR. LEE: Thank you, Your Honor.

THE COURT: If you all will meet and confer between now and Monday or Tuesday if you can and then get me something by Thursday and y'all will have it by Friday.

MS. WEN: Okay. Thank you, Your Honor.

THE COURT: You bet.

Give me one second.

(Conference between Ms. Miles and the Court.)

THE COURT: Ladies and gentlemen, I'm trying to figure out what works best for you all and for us. We have the courthouse Christmas lunch today, which, believe it or not, they actually invited me to this year. So I think it would be -- for me to play my part in that, it'd probably be best for me to be there at 11:30. If you all will be back by 12:30 or 12:45, whichever

is -- 12:45 would probably be easier on you all at this time to get stuff done. We'll start back up at 12:45 with the next claim term if that works. Unless you all would like to keep going now and do something different, but that --

MR. LEE: That's fine with us, Your Honor.

THE COURT: Okay. We'll see you back at 12:45.

(A break was taken from 11:23 to 12:50.)

THE BAILIFF: All rise.

THE COURT: Thank you. You may be seated.

What's up next?

MS. WEN: I just wanted to actually return to the capacitance structure very quickly if I could.

THE COURT: Sure.

MS. WEN: We did some Googling of our own over the lunch break.

(Laughter.)

MS. WEN: And wanted to just provide some evidence that Mr. Lee said didn't exist, specifically that 397 of about 1,090 hits on Google Scholar for a capacitance structure are from before 2006 and we would be happy to provide more color in any supplemental submission that we provide to the Court, for example, the Thursday submission that you were talking about before we broke for lunch.

THE COURT: Okay. Okay. Let's move on then to the claim term precharging means for precharging the capacitance

structure to a predetermined voltage prior to a write operation for the second line of memory cells.

MS. WEN: Yes. And I believe, Your Honor, Josh sent an e-mail just before the hearing and we are prepared to agree to that construction as well. I think Mr. Lee mentioned that Intel was --

MR. LEE: That's correct, Your Honor.

THE COURT: Then Josh did a great job drafting it. Great. Thank you.

Okay. So the construction that we are going to put in -- that we're going to enter in our order is the one that Josh sent to you with the agreement of the parties.

So the next claim term we have up is first coupling means for coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells.

MS. WEN: Yes.

Can we jump to Slide 115? Or I can just click through.

All right. So there are two coupling functions at issue here. The first is the first coupling means for coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells. And I'd like to discuss this kind of at the same time as the second coupling means for coupling the second supply line to the first capacitance structure during the write operation for the second

12:52 1 line of memory cells. I think the parties sort of briefed them
12:52 2 in concert as well. And I especially want to do this because
12:53 3 VLSI has proposed the same structure for both coupling
12:53 4 functions, because, as we will show, the specification
12:53 5 explicitly states that the switching circuit or a switching
12:53 6 circuit or equivalence of that switching circuit performs both
12:53 7 of these two coupling functions exactly as recited in the
12:53 8 claim.
12:53 9 So as it says on Slide 117, Intel's proposals for
12:53 10 structure for both of these terms ignore the switching circuit
12:53 11 entirely, and they attempt to justify this by saying that
12:53 12 switching circuit is not properly structured because it is a
12:53 13 means plus function term. And that is not borne out by the
12:53 14 evidence which I'll talk about shortly, and also want to talk
12:53 15 about why Intel's proposed structures are also specifically
12:53 16 flawed outside of the fact that they ignore the switching
12:53 17 circuit.
12:53 18 So to take a little bit of a step back, the Federal
12:53 19 Circuit requires that when you're construing a means plus
12:54 20 function term, the specification must be read as a whole to
12:54 21 determine the structure. And in construing terms used in the
12:54 22 patent claims, it is necessary to read all portions of the
12:54 23 written description and not just some portions of it.
12:54 24 Specifically identifying corresponding structure requires the
12:54 25 Court to examine both the drawings in the abstract and the

patent's written description. And this is relevant because -- jumping ahead to Slide 121, this is relevant because the abstract discloses that the switching circuit performs the claimed coupling functions. It also performs a decoupling function, but we'll get to that a little bit later. So as you can see, the -- in Slide 122 the first coupling function reads: Coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells. And the abstract specifically discloses that for the case where the second line of memory cells is selected for writing, a switching circuit couples the power supply terminal to the first power supply line.

The same is true for the second coupling means. The claim language for the second coupling means is highlighted in green -- or I'm sorry -- underlined in green, and it reads: Coupling the second supply line to the first capacitance structure. In the abstract it says, where the second line of memory cells is selected for writing, a switching circuit...

If you jump to the green underlined text, it says, couples the second power supply line to the first capacitance structure.

So, as you can see, the abstract specifically states that the switching circuit performs this function. It's not just the abstract though. Later in the specification it also says that a switching circuit that has transistors that -- and

there's an extra "that" in there -- couple the first power supply terminal to the first supply line and couple the second power supply line to the first capacitance structure.

And on Slide 124 you'll see that we once again underline the text of the first coupling function in blue and the text of the second coupling function in green.

In addition to these disclosures, the figures of the patent also disclose that a switching circuit performs the coupling functions. As our expert Dr. Conte declared, transistors of the type depicted here, for example, Transistor -- number's not very clear -- but Transistor 54, I believe -- transistors of the type depicted here can be used to couple and decouple components on demand and are examples of a switching circuit.

THE COURT: Don't -- I have a couple of questions for you.

MS. WEN: Sure.

THE COURT: Don't leave that slide which is a slide that shows Figures 2 and Figures 3.

MS. WEN: Yeah.

THE COURT: Why should I not be concerned that switching circuit is functional and not structure?

MS. WEN: Sure. So we provided -- well, first, when determining, as -- we just went through this, but when determining whether a term is a means plus function term, you apply the test of whether first it includes the words "means,"

which it does not.

THE COURT: I got that.

MS. WEN: Yeah. And then, second, you consider whether a person of ordinary skill in the art would understand that the term is structure.

THE COURT: Okay. Well, why don't you tell me, though, why it's not functional?

MS. WEN: Do you mean --

THE COURT: Why you -- why it's -- why don't you explain to me here why I should not be concerned that it is functional?

MS. WEN: So I don't think -- so we provided an expert declaration that explains that a person of ordinary skill in the art would understand the meaning of a switching circuit upon reading the disclosure of the '485 patent. Specifically that example's switching circuits can include switch circuits, switching circuits, switches and transistors configured to act as switches. And the Federal Circuit has held that if a claim term is used in common parlance or by persons of skill in the pertinent art to designate structure, it is not necessarily a means plus function term even if the term identifies the structures by their function.

THE COURT: Yeah. I got that. Here -- I don't mean to be impolite.

MS. WEN: No. No. No.

THE COURT: But other than your expert who says what he

says -- and I have my reservations about the value of experts making those statements because Intel is capable of getting someone who will say exactly the opposite and they obviously are both skilled in the art. I'd like to hear your best argument about why I shouldn't be concerned that a switching -- and if Mr. Lee thinks I'm barking up the wrong tree and they're not taking this position, I won't pester you with it, but I'm guessing Mr. Lee is -- agrees with my concern.

MR. LEE: We do, Your Honor.

THE COURT: Okay. And so I want to -- I would like to hear your best argument as to why a switching circuit is -- I shouldn't be concerned that it's functional.

MS. WEN: Okay.

THE COURT: And I got that you have an expert that says what one skilled in the art would say, but I'd like to hear your best argument.

MS. WEN: Right. So in addition to our expert, we also wanted to point out that in Intel's invalidity contentions they state that switching circuit -- well, the use of switching circuits in memory devices, including to decouple a column of memory cells from a first power supply --

THE COURT: You need to slow down, please.

MS. WEN: Sorry.

Including to decouple a column of memory cells from a first power supply terminal and couple that column of memory

cells to a second circuit node was well-known in the art prior to the alleged invention of the '485 patent.

THE COURT: Well, again, I think Mr. Lee will do a great job speaking for himself or whoever's going to argue this, but I don't think -- I don't think the quote that you just gave me does anything to make me not think it's not functional. The switching circuit -- the use of switching circuits in memory devices is performing that function.

MS. WEN: So is your concern that it says switching in the term?

THE COURT: Yes.

MS. WEN: Okay. I think that a term can be functional without being a means -- are you -- without being a means plus function term.

THE COURT: That is -- I will confess I don't know that I've thought that through, but I do -- I am concerned that -- and the Intel folks can add to that, but I am concerned that you all are proposing switching circuit as the structure, and I'm -- and what I'm saying is I don't believe it is a structure. I believe it might be function. And so you are kind of going at it from the position of, is this a -- you know, a means plus function term? I think we are in agreement that it is what we are fighting over because you guys have agreed to the function. What we're having a hard time here -- I'm having a hard time. You're probably doing great and I'm

not following you -- is that your advocacy of a switching circuit as the structure strikes me as maybe -- regardless of whether Intel is right or not in what they've suggested, I'm concerned that your suggestion of switching circuit is not correct because it is -- because it is functional rather than structural, and that's what I'm trying to get you to help me with here.

MS. WEN: I see. Okay. Well, I would start by saying that a circuit is a structure. I think we're on the same page about that. It says switching circuit and we're in agreement at least that circuit is structure.

THE COURT: Yes.

MS. WEN: Okay. I would say that the patent discloses examples of a switching circuit specifically in these figures.

THE COURT: Well, yeah. In Figures 2 and -- Figure 2 for sure and --

MS. WEN: Yeah.

THE COURT: You know, because we've got Transistors 52 and -- and 44, but, you know, you all have taken the position, I believe, that Intel is wrong with what they're suggesting, but isn't it true that here Transistors 52 and 44 are off, meaning the power supply terminal is not connected to the first power supply line? I think I have that right, don't I?

MS. WEN: Are you referring to the write operation? What's occurring during the write operation?

01:03 THE COURT: Yes.
01:03 MS. WEN: So --
01:03 THE COURT: During writing to the memory cells in Column 13, 52 and 44 are off. They're not connected.
01:03 MS. WEN: So okay. So we agree with Intel that during the write operation for the second line of memory cells.
01:04 THE COURT: And they're on then when writing the memory cells in Column 15, right?
01:04 MS. WEN: Column 15, yeah. So we agree with Intel that when writing to the line of memory cells in Column 15 Transistor 44 is decoupled.
01:04 THE COURT: So doesn't -- isn't Intel's proposal -- I mean, the way they have it, doesn't that support Intel's position that their structure -- their proposed structure is correct?
01:04 MS. WEN: I see. I don't think we disagree with Intel in terms of the specific transistors that are disclosed in Figures 2 and Figure 3.
01:04 THE COURT: Okay.
01:04 MS. WEN: I'm sorry. Figures 2 and 3 as performing this function. We -- where we disagree is I think we're taking the position that those specific transistors are not the only structure that the patent discloses as capable of performing the function.
01:05 THE COURT: What else is there?

01:05 MS. WEN: The switching circuit and of course the equivalence of Transistors 52 and 44.

01:05 THE COURT: Okay. And I'm sorry I interrupted you, but -- so if you wanted to pick back up where you were.

01:05 MS. WEN: Sure. So just going back to the means plus function point, Intel never proposed switching circuit for a construction. The term "switching circuit" appears in Claim 1 and Claim 12, and Claim 12 has been asserted since we filed our complaint in April. Claim 1 has been asserted since our preliminary infringement contentions were served on Intel on July 22nd. When the parties exchanged claim terms for construction, Intel never suggested that a switching circuit was a means plus function term. And after we proposed a switching circuit as structure for these decoupling and coupling terms, Intel again did not raise that switching circuit should be construed for Claims 1 and 12.

01:06 THE COURT: Okay.

01:06 MS. WEN: And another example of the positions that Intel has taken include another page in their invalidity contentions in which they state that a person of ordinary skill in the art would have understood how to successfully use the switching circuit to switch between voltages.

01:06 THE COURT: Okay. Anything else?

01:06 MS. WEN: Yes. So I want to talk about briefly why Intel's specific proposals are flawed. Like I mentioned, it

excludes the embodiments -- it excludes embodiments, including specifically the switching circuit, and we disagree that structure should include the additional function of coupling power supply voltage VDD and Conductor 35 as well as the function of coupling power supply voltage VDD and Conductor 67 because the claimed function here is as stated in the claim, which is coupling the power supply terminal in the first power -- coupling the power supply terminal to the first power supply line during the write operation for the second line of memory cells.

Another reason why we disagree with Intel's proposed structure for the first coupling term is because it includes a clamping circuit which does not perform the first coupling function.

THE COURT: What does? A reference volt? What does perform the coupling function?

MS. WEN: The switching circuit is our proposal.

THE COURT: Okay. And I may have misunderstood. I think when I was -- I think VLSI was taking the position that a clamping circuit is not needed, right?

MS. WEN: Yes.

THE COURT: Because a reference voltage could be used?

MS. WEN: Yes.

THE COURT: Okay. If that were true, if you are correct, what evidence do you have that a person of skill in the art

would understand how to implement the referenced voltage in the same way as the clamping circuit that is -- that Intel proposes and that's disclosed?

MS. WEN: Sure. So let's get to -- so our expert has explained that the patent's disclosure of -- in another embodiment, a reference voltage can be used essentially means that a person of ordinary skill in the art would understand that instead of coupling --

Can I have Figure 2 of the patent? '485 patent. Or maybe I'll find it here first so I can point it out.

Okay. So this is the clamping circuit here that Intel contends is performing the first coupling function, and this right here is coupled to something that is labeled VDD which, as you've seen in Intel's other slides, is just a big purple block that encompasses all the VDD nodes or VDD structures -- well, VDD references on this figure.

And so if -- so the patent discloses that instead of being coupled to the power supply terminal, the big -- the purple block with VDD, this would be coupled to another voltage source like a reference voltage source. So it was providing a reference voltage.

THE COURT: And where is that disclosed in the patent?

MS. WEN: It is disclosed in that sentence where it provides that a clamping -- that a reference voltage can be used instead.

THE COURT: Is that in the patent or is that in your expert's declaration?

MS. WEN: I think it's in the patent. The patent specifically says --

THE COURT: I know that there is a reference to a reference voltage. And so where's it at?

MS. WEN: In other embodiments the clamping circuit can be different. For example, in another embodiment -- and we can skip this part -- a reference voltage can be used.

THE COURT: And which slide are you on?

MS. WEN: I'm on Slide 138. I'm sorry.

And this is referring to Column 3, Rows 55 to 58 of the '485 patent which is Exhibit 2.

And I just want to make an additional note which is that Intel has not at any point contended that the clamping circuit is purely functional but it follows the same nomenclature as the switching circuit.

And if it would be helpful to the Court, I think we could go back and provide you with examples of switching circuits being used in the art.

THE COURT: And are the parties in agreement as to what the first coupling means is? Which portion of --

MS. WEN: The function?

THE COURT: I'm saying -- I mean -- that was a bad question. Are you in agreement with regard, for example, as to

which transistors are -- make up the first coupling means?

MS. WEN: Well, not the clamping circuit but the specific transistors in the figures. Yes.

THE COURT: Okay. Okay. Did you have anything else you wanted to add?

MS. WEN: I wanted to move to the second coupling function which should be quick.

THE COURT: I'm sorry. I just couldn't hear you.

MS. WEN: I'm sorry. I wanted to move to the second coupling function because we were just dealing with them together.

THE COURT: Yes, ma'am.

MS. WEN: Similar points. We think that Intel's proposed structure excludes the switching circuit. It attempts to add additional functions this time coupling Conductor 39 to Conductor 37 and, secondly, coupling Conductor 69 to Conductor 71.

And the Federal Circuit has held that when multiple embodiments in the specification correspond to the claimed function, proper application of Section 112, Paragraph 6 generally reads these claim elements to embrace each of the embodiments.

THE COURT: Okay.

MS. WEN: So that's all.

THE COURT: Mr. Lee, will you be speaking?

01:13 MR. LEE: I will, Your Honor.
01:13 THE COURT: Very good.
01:13 MR. LEE: So, Your Honor, if I could take you in our Markman slides to Slide 24 which I'll also put on the screen.
01:13 THE COURT: Okay. Give me one second.
01:13 MR. LEE: Sure.
01:13 THE COURT: I'm knee deep in --
01:13 MR. LEE: And it only gets worse.
01:13 (Laughter.)
01:13 THE COURT: So let me -- I believe I'm with you. And did you say Page 24?
01:13 MR. LEE: Page 24.
01:13 THE COURT: Okay. Give me one second. I'm with you.
01:13 MR. LEE: Okay. So this is just Claim 17, and I agree with Ms. Wen that we can take these two together and I think I can take them together and make it a little bit more efficient.
01:13 There are two problems with the argument that VLSI has offered, and these are the problems. There's no disagreement these are Section 112, Paragraph 6 claims. There's no disagreement as to the function. So the only disagreement we have before you is, what's the structure? And this is a case where the structure that performs this function is very specifically described in Figures 2 and 3. And harkening back, without being redundant to our discussion of why you have Section 112, Paragraph 6 and to your question to VLSI, you

know, can you just claim this functionally? The answer is no, not yes.

So the two problems are this: The structure that is disclosed is quite specific, and switching circuit is not part of the disclosure in sufficiently specific terms to satisfy Section 112, Paragraph 6.

THE COURT: And correct me if I'm wrong, but the structure -- as best I could tell, the structure that Intel has provided is essentially just taking a section, as it were, of Figure 2 and typing it out as to what is contained in that particular section of Figure 2 as to what you believe that coupling means is, correct?

MR. LEE: Correct. So both for the first coupling means we've identified the transistor and the clamping --

THE COURT: Yes, sir.

MR. LEE: For the second just the transistor and --

THE COURT: Basically you've taken what was in the figure of the patent and just, for lack of a better word, grammar -- you've turned it into words. You haven't added any -- if I were to look at that figure -- if a person skilled in the art were looking at the figure, they would understand where this structure you proposed came from by looking at that figure, correct?

MR. LEE: Exactly and precisely, and as I said -- well, we dealt with capacitance structure although that may have been

irrelevant. You know, if Your Honor directed us to, we probably could take what the specification says specifically and simplify it before for the jury is charged, but we felt -- if I go to Slide 25.

THE COURT: Okay.

MR. LEE: What we'd have on the structure is just what Your Honor said. So it's -- Part 1 is Figure 2. Part 2 is for Figure 3.

THE COURT: Right.

MR. LEE: And we just tried to take it verbatim. And I don't think that there's any disagreement that for the first coupling means there is the transistor and the clamping circuit. There's a disagreement about whether the clamping circuit should be part of it, and I'll come to that. For the second -- if I go to Slide No. 26, this is the second coupling means and there are a lot of words on the slide, Your Honor, but most of them we agree to. Most of them are just the claim, the function, and here's the disagreement, and as Your Honor suggested, we've just taken what is in Figure 2 or, alternatively, Figure 3, and VLSI has just offered the switching circuit.

THE COURT: And is there any reason why, if I were to use the structure that you proposed for each, I couldn't make it clear that, for example, the transistors could be NMOS or PMOS, or do you take the position that the patent only covers a

specific type of transistor?

MR. LEE: I think the disclosure here is just a transistor. So if Your Honor said a transistor, that would be fair.

THE COURT: Okay.

MR. LEE: Okay. And I think that literally are -- is the words, and if I move to -- let me skip 27 and go to 28.

So this is, as we said, if the patent is specific as what the first coupling means is and what the second coupling means are -- is one's a transistor alone. The second coupling means the other is the first coupling means in the clamping circuit.

Now, we do have a disagreement about whether the clamping circuit should be included, and if I go to Slide 29, you'll see that we've tried to do, Your Honor -- again, as I said, the key here is, what did they say, right, when they claimed this functionally? And what they say is what is providing this coupling is this Transistor 52 and the Clamping Circuit 48 and 50. The mere fact that the clamping circuit can perform other functions doesn't mean it's not helping perform this function. And the specification itself says that that's precisely what is occurring. There is an argument that -- by VLSI about Transistor 52 and a suggestion that it decouples the first power line. So we're up here. If Your Honor looks at the portion of their argument, they're talking about a situation where you're writing to Column 13 and you want the voltage to

01:19 go down. Our example in Claim 17 is when you're writing to the
01:19 second column and you're not writing to Column 13. So if
01:19 that -- that structure, we suggest, is very specific, and if I
01:19 go to Figure 3, Slide 30, in the interest of time, it's the
01:19 same. The coupling is performed by the transistor and the
01:19 clamping circuit that's in 100 and 102, Transistors 100, 102,
01:19 and the decoupling is performed by the transistor shown with
01:19 the X.
01:19 Both Figures 2 and Figure 3 are consistent and they're
01:20 very specific and they say, here's the function. Here's in the
01:20 one case the transistor and the clamping circuit that performs
01:20 that function. In the second here's the transistor that
01:20 performs that function. The only response is, no. No. It
01:20 could also be a switching circuit. And what they rely upon, if
01:20 I go to Slide 33, is the statement from the specification. And
01:20 there are a couple of different important things about this.
01:20 The first thing is the switching circuit doesn't provide you
01:20 with any structure. Whether you call it a means plus function
01:20 limitation is not particularly relevant to this discussion.
01:20 The question is, does it disclose specific structure that makes
01:20 it something other than functional? And it doesn't.
01:20 THE COURT: You said that -- I'll need to ask Ms. Wen when
01:21 she gets back -- you said it better than I could ask her the
01:21 question. So when --
01:21 Ms. Wen, when you get back up here, what Mr. Lee said was

what I was trying inartfully to ask you about and ask you -- I'm going to ask you to rebut the argument he's making right now because he's saying it better than I could, but I -- I mean, Mr. Lee, you're making the point I was concerned about.

MR. LEE: And, Your Honor, there are only two places where the patent refers to the switching circuit. One is the specification which is on Slide 33. And if I flip to Slide 34, the other is in the abstract.

Now, these actually paraphrase what ultimately ends up in Claim 1, not the claim we're looking at now. And I think there are three important points to make. If I go to Slide 35, the idea of an abstract or some general portion of the specification, paraphrasing Section 112, Paragraph 6 language, is not a new one. And the argument that's being made to Your Honor on the switching circuit has been made analogously in other cases, and the courts have said, no. No. No. You can't do that. And the reason is they're trying to avoid -- the courts are trying to avoid dysfunctional claiming. That's Problem No. 1.

Problem No. 2 is that the structure for decoupling in the first sentence and the second sentence are here very specifically disclosed and never called a switching circuit. They're called the transistors clamping circuit or the transistors and no one ever calls them a switching circuit.

And then No. 3, the switching circuit is part of a

separate claim with separate limitations, other limitations that go along with it that don't amplify the discussion we're having here at all.

But I think at the end, Your Honor, no one disagrees it's Section 112, Paragraph 6. No one disagrees that there's a function. No one disagrees that Figures 2 and 3 are the disclosed embodiments of the invention, and that has special meaning for means plus function limitations, and no one disagrees as to what's disclosed. The only disagreements are should a clamping circuit be included? That's what the patent says. Can the switching circuit in general articulation save it? And the answer is no.

THE COURT: Thank you, sir.

MS. WEN: Could you please jump to Slide 124?

Thank you.

So to respond to the question of whether a switching circuit discloses structure, I would point out in the patent, and Mr. Lee was just talking about this section of the specification as well. This is Slide 124, and underlined in red it says, a switching circuit has transistors that couple the first power supply terminal to the first power supply line. So the patent does specifically disclose a switching circuit with transistors which Mr. Lee just stated neither of the parties dispute are a structure. He also noted, I think, that it doesn't matter whether Intel is relying on means plus

01:24 function claiming with respect to their switching circuit
01:24 argument. I think it does matter. It matters first because
01:24 the authority that they rely on to say that you can't point to
01:24 functional language in the specification specifically deals
01:24 with means plus function terms. And I -- and we, as I stated,
01:25 disagree that switching circuit is purely functional. The
01:25 patent clearly states that a switching circuit has transistors.
01:25 The figures disclose that there are transistors that operate as
01:25 switches during the write operation. And so we would say that
01:25 a switching circuit, if the Court would like a general
01:25 definition, is a class of structures that has switches that
01:25 open and close.
01:25 And so I also want to respond to Mr. Lee's argument about
01:25 the clamping circuit. The clamping circuit is not required to
01:25 perform the first coupling function. As we -- as I stated
01:25 earlier, the patent specifically contemplates that in other
01:25 embodiments the clamping circuit is not coupled to the power
01:25 supply terminal but is, rather, coupled to a different
01:25 reference voltage. And here if you look at the figures
01:25 themselves, you can see that Transistor 52, which is coupling
01:25 the first line of memory cells to the power supply terminal,
01:26 can do so with or without Clamping Circuit 48. So Transistor
01:26 52 alone is sufficient to perform the coupling function, the
01:26 first coupling function in this figure.
01:26 THE COURT: Would you say that again?

01:26 MS. WEN: Yeah. So this figure clearly -- so Intel is arguing that to perform the first coupling function you need both this Transistor 52 --

THE COURT: In Clamping Circuit 46?

MS. WEN: Yes.

THE COURT: Yes.

MS. WEN: And this figure clearly shows that Transistor 52 alone would be sufficient to couple to the power supply terminal, and this is buffered by the disclosure in the patent of a clamping circuit that is not coupled to the power supply terminal.

THE COURT: Anything else?

MS. WEN: That is it for me.

THE COURT: Mr. Lee?

MR. LEE: Two very quick points, Your Honor.

To end where -- to start where Ms. Wen ended, the question is not what is sufficient to perform the function. The question is what's disclosed to perform the function because that's how they define their invention and avoid the prior art. And if you look at Column 3, Lines 48 to 58, you'll see that the clamping circuit is part of what is performing this function.

Second to last --

THE COURT: Give me -- let me get there real quick.

MR. LEE: Okay. If I go to 48 of Column 3.

01:27 THE COURT: Okay.

01:27 MR. LEE: Well, actually, let's go over to Column 3 -- Column 4 actually. Let's go to Column 4 first.

01:27 THE COURT: Okay.

01:27 MR. LEE: And Line -- come down, Mr. Lee.

01:28 THE COURT: I've actually got the patent here in front of me too.

01:28 MR. LEE: So, Your Honor, here is a portion describing specifically what the clamping circuit's doing and how it is affecting the -- what is coming out of the supply terminals. This is part of what they're describing as the coupling means. And that's why the clamping circuit should be included.

01:28 THE COURT: And what lines in Column 4?

01:28 MR. LEE: It's 48 to -- so it starts as illustrated in Figure 2 and it goes on.

01:28 THE COURT: Got it. Let me read that real quickly.

01:28 MR. LEE: It says the Clamping Circuits 38 and 46 function to limit the voltage drop on Conductors 35 and 39 to a predetermined minimum voltage. The supply voltage is only reduced on the columns being written to. The reduced supply voltage functions to improve the write margin of the selected cells while maintaining the cell stability of the unselected cells. That's part of the coupling function, and the clamping circuit helps to control that.

01:29 The last point -- could I have Slide 33, Mr. Lee?

01:29 THE COURT: Well, and you might want to address the portion of the patent -- I've forgotten where Ms. Wen said it was -- that talked about reference voltage being able to be used in -- being disclosed as being able to be used as opposed to a clamping circuit.

01:29 MR. LEE: It may be that it can be used without a clamping circuit. The question here is what is disclosed as the specific means, and this is what's disclosed with the clamping circuit in every circumstance.

01:29 THE COURT: And is it your position that given that it is a means plus function claim I have to put in -- I have to stick with what the function that's disclosed in this part of the specification?

01:29 MR. LEE: It is -- yes. What the function is and then what is disclosed to the spec to perform that.

01:30 THE COURT: To perform that function. Yes.

01:30 MR. LEE: Slide 33. Your Honor, here is the difference, and I may have gone too quickly when I said that the switching circuit was sort of paraphrase in Claim 1. The reason you don't have the same problem we had with the capacitance structure or some other theory, there's a switching circuit which in isolation has a problem that we talked about now. But the claim says it has transistors and then it specifically says where they're located, what they're connected to and how they -- how those connections work. So there are a legion of

cases that say if you have a term but by defining, you know, what it is, here a transistor, but where it's located, what it's connected to, you're providing the structure in words. That's the difference. But that switching circuit, if you look for the description of the coupling and decoupling means at Figures 2 and 3, we can search forever and you won't see the switching circuit suggested as the structure.

Thank you, Your Honor.

THE COURT: Anything else from VLSI?

MS. WEN: All right. So very quickly. Mr. Lee said that the question is what is disclosed to perform the function, and, like we said, the switching's the patent, the written description, the abstract. The preferred embodiments repeatedly state that a switching circuit is what performs these functions to the letter. And this statement in the specification it clearly discloses that there are transistors within the switching circuit. I wasn't really sure what Mr. Lee was saying about the transistors being separate from the switching circuit or not being within the switching circuit. This clearly contemplates a switching circuit which couples the first power supply terminal to the first power supply line and couples the second power supply line to the first capacitance structure and the switching circuit has transistors. And --

THE COURT: And that's Column 6, Lines somewhere around 50

01:32 through 54?
01:32 MS. WEN: Yes. That would be 47 through 58 I believe.
01:32 THE COURT: Yeah. That's the full paragraph. Yes.
01:32 MS. WEN: Yeah.
01:32 THE COURT: Begins at 47. Yes, ma'am.
01:32 MS. WEN: Yes.
01:32 So this is -- it's very clear like both in the claims and in the specification that it's the switching circuit that performs the function. And I don't have the claims on these slides, but Mr. Lee pointed out to you the particular claims that contain the switching circuit terminology which includes, I believe, Claim 1 and Claim 12. And I want to reiterate that you can talk about circuits in terms of their functions without having them be means plus function terms. And a person of ordinary skill in the art would understand switching circuit as structure, and we are happy to submit examples of that if the Court would like to see it.
01:33 THE COURT: Anything else?
01:33 MS. WEN: No.
01:33 THE COURT: Mr. Lee?
01:33 MR. LEE: Nothing, Your Honor.
01:36 (Conference between the Court and Mr. Yi.)
01:39 THE COURT: The Court is going to find that the construction for first coupling means for coupling the power supply terminal to the first power supply line during the write

01:39 operation for the second line of memory cells will be the
01:39 agreed function is coupling the power supply terminal to the
01:40 first power supply line during the write operations for the
01:40 second line of memory cells. The structure will be Transistor
01:40 52 and Transistor 96 and equivalence of either.
01:40 With respect to second coupling means for coupling the
01:40 second supply line to the first capacitance structure during
01:40 the write operations for the second line of memory cells, the
01:40 agreed function is coupling the second supply line to the first
01:40 capacitance structure during the write operation for the second
01:40 line of memory cells. The structure will be Transistor 54 and
01:40 Transistor 94 and equivalence thereof.
01:40 We will turn now to claim term decoupling means for
01:40 decoupling the first power supply line from the second line of
01:40 memory cells during the write operation for the second line of
01:41 memory cells.
01:41 It is my inclination -- I will tell VLSI my inclination is
01:41 that this is indefinite. I don't need to hear from Intel, I
01:41 don't think, unless I just need to hear from them after you --
01:41 whoever speaks for VLSI, but if you -- do what you can to
01:41 persuade me why I'm wrong whoever's going to speak for VLSI.
01:41 Give me one second.
01:41 (Conference between the Court and Mr. Yi.)
01:42 THE COURT: On the last two claim constructions I gave, I
01:42 used the word "and" between the transistors. It should be

"or." It can -- it does not -- it's not required to have both. And so if that wasn't clear, I want that to be clear on the record.

So, yes, ma'am. If you would take up the decoupling means for decoupling the first power supply line.

MS. WEN: Sure. And I won't rehash too much of what we've said, but I like to start that Intel has the burden to show by clear and convincing evidence that the specification --

THE COURT: I would -- I would skip over that.

MS. WEN: All right. Great.

THE COURT: I'm pretty good with the --

MS. WEN: All right. So, again, the switching circuit is structure. Mr. Lee said that in Claim 1 -- I don't have it here.

Can we have Claim 1?

THE COURT: I'm with you on Claim 1.

MS. WEN: Okay. All right. So it says a switching circuit -- a switching circuit has transistors that connected between the first power supply terminal, et cetera. Mr. Lee said that the reason that they didn't propose switching circuit as a means plus function term was that the transistors make it okay. So the transistors are structure. We agree that the switching circuit discloses structure, and because the switching circuit discloses structure and it also discloses specifically that the switching circuit performs the decoupling

function --

Can we go back to the slides?

It is our position that the patent clearly discloses again a switching circuit that has transistors that, when the second line of memory cells is selected for writing, decouple the first power terminal from the second line of memory cells.

In addition, it states that --

THE COURT: Why don't you do this? This will probably be the most -- thing most helpful to you. I think I'm correct, and Josh can tell me if I'm -- if this is where we got to yesterday, but I think it'd be most helpful for you to go to the Figure 2 is what we looked at, right, and if you would go to Figure 2 and explain to me, you know, basically how the first power supply terminal could be coupled with the first power supply line, and by coupled, that doesn't make sense to me. And so that would be -- that would be helpful to you.

MS. WEN: Okay. So I think how I would explain it is here we have the first power supply line and here we have the second power supply line. I'm just using Intel's figure. And here we have the power supply terminal. So the patent discloses that the first power supply line is coupled to the power supply terminal. It also discloses that the second line of -- the second power supply line is coupled to the power supply terminal. And so the patent additionally discloses that the second line of -- the second power supply line becomes

decoupled from the power supply terminal. And so when this decoupling action occurs, it is effectively also coupled from the first power supply line.

Maybe that wasn't clear.

THE COURT: Well, what is the difference in your switching circuit from the first power supply terminal?

MS. WEN: Could you --

THE COURT: I may not be getting this right, but my thinking was that basically the switching circuit is the same thing as the first power supply is what's -- aren't you arguing that your switching circuit is what's in the purple box?

MS. WEN: No. No. No.

THE COURT: Okay.

MS. WEN: So the switching circuit corresponds in this figure to these transistors.

THE COURT: Okay. And that's -- and I think maybe this is what we were talking about yesterday is are you all in agreement that the purple box should not also include that?

MS. WEN: Should not also include a switching circuit?

THE COURT: Yeah. Where -- as the --

MS. WEN: Okay. So the purple box is the power supply terminal.

THE COURT: And that would not include the circuit that's below it?

MS. WEN: No. It would not.

01:47 THE COURT: Okay.

01:47 MS. WEN: So we have this power supply terminal which is --

01:47 THE COURT: Okay.

01:47 MS. WEN: -- coupled to both the first power supply line --

01:47 THE COURT: Okay.

01:47 MS. WEN: -- and the second power supply line.

01:47 THE COURT: Right.

01:47 MS. WEN: And it's coupled through switching circuits.

01:47 THE COURT: Okay.

01:47 MS. WEN: For example, this transistor.

01:47 THE COURT: So that wouldn't be -- as a non technical person, you're getting to where my inartful question is. So it would not include -- let me get to Figure 2. It would not include -- I guess 42 -- it would not -- it stops at the bottom line of where the purple is and doesn't include anything below it to be the power supply?

01:48 MS. WEN: Right. So the power supply terminal basically corresponds to these VDDs.

01:48 THE COURT: Okay.

01:48 MS. WEN: And just those.

01:48 THE COURT: And does not include anything else?

01:48 MS. WEN: No.

01:48 THE COURT: Okay.

01:48 MS. WEN: Okay. So with that understanding, you can see that the first power of supply line is connected to the power supply terminal through the switching circuit transistor.

01:48 THE COURT: Okay.

01:48 MS. WEN: And the second line of memory cells -- I'm sorry. The second power supply line, which is not labeled here, is coupled to the same power supply terminal through a different switching circuit transistor right here. And so when you decouple this second power supply line from the power supply terminal, you are effectively decoupling it from the first power supply line, if that makes sense.

01:49 THE COURT: Yes, ma'am. I mean, I hear what you're saying. I don't know that I agree with it, but it makes sense.

01:49 MS. WEN: So that's why we're saying that it is not indefinite that the patent clearly discloses that these switching circuit structures decouple the first -- I'm sorry. The -- yeah. The first power supply line from the second power supply line.

01:49 THE COURT: And if I have Intel's -- if I understand what Intel is arguing, it is that the specification does not describe coupling the second line of memory cells to the first power supply. That's Intel's position, correct?

01:49 MS. WEN: Yes. They are arguing that the claim does not disclose the first power supply line being directly coupled to the second power supply line.

01:50 THE COURT: Their position is that the specification only discloses coupling the first line of memory cells to the first power supply and the second line of memory cells to the second power supply, correct?

01:50 MS. WEN: Yes.

01:50 THE COURT: And you -- if you can explain to me why they're incorrect.

01:50 MS. WEN: So I -- they are -- what's a good word for this? They are kind of ignoring the fact that the first power supply line is coupled to the power supply terminal. The second power supply line is also coupled to the power supply terminal. So when you decouple one -- for example, when you decouple the second power supply line from the power supply terminal, you are decoupling the first power supply line from the second power supply line.

01:50 THE COURT: Unfortunately my problem here is with that -- is with our technology. My screen is so bad that I can't see far enough to see that, and I -- and the screen is bad. I can't see this. So I'm trying to follow along with what you're saying.

01:51 MS. WEN: All right. Let me --

01:51 THE COURT: Maybe we have this. If you can tell me where this slide is that you're working off of and you can give me a hard copy of that.

01:51 MS. WEN: It is -- let me grab that slide number back

actually. Slide 149.

THE COURT: Okay. Now, using that, if you can just articulate for me exactly what the purple square is going around by using the numbers.

MS. WEN: Yes. So there aren't any numbers associated with the power supply -- with the purple box. You see the VDD and the little circle below it and then another VDD and a circle below it.

THE COURT: Yes, ma'am.

MS. WEN: Yes. Those four VDDs correspond to the power supply terminal that we're talking about.

THE COURT: So are the power supply terminals that -- is the power the VDD that attaches to Line 1 and the VDD that applies to Line 2, are those not separate power supplies?

MS. WEN: No. It's the single power supply terminal, and this is the position that both parties have taken throughout the course of the briefing. Intel suggested in their reply briefing that these VDD -- these separate VDD reference are somehow separate nodes, but that's not consistent with what they've been arguing before that or how they presented the power supply terminal today. And so our position is that the first power supply line and the second power supply line are both connected to the same power supply terminal such that when you decouple one from the power supply terminal, you're decoupling the other supply line as well from the initial --

from the first power supply line.

THE COURT: Why don't we -- Mr. Lee, who's arguing on your side?

MR. LEE: I am, Your Honor.

THE COURT: Why don't we hear from him on that specific issue and then you're welcome -- I'll have you get back up on anything else you want to say, but that's what I really care about.

MR. LEE: Your Honor, if I could go on our slide to Slide 37 --

THE COURT: Okay.

MR. LEE: -- directly.

And just to put it in context, so the function that's described is decoupling the first power supply line from the second line of memory cells, right? That's what we're focused on, that phrase. So in order to decouple the first power supply line from the second line of memory cells, they have to have been coupled to each other in the first instance.

If I take you then to our Slide 40, Your Honor, which is the diagram that you were looking at before, the power supply is up here. These are separate nodes from the power supply, but the claim of the case is not referring to the power supply or power terminal. It's talking about the supply line.

THE COURT: That was the way I was taking it too. I know I was not being very articulate when I was asking Ms. Wen, but

that is my concern here.

MR. LEE: And there is a second supply line that's supplying voltage to the second column of cells, but --

THE COURT: But not from that first power supply?

MR. LEE: Right.

THE COURT: Yes.

MR. LEE: That's why we have the transistor up here to decouple. So the first power supply line is never coupled to the second line of memory cells. Because it's never coupled, it can't be decoupled.

THE COURT: Decoupled.

MR. LEE: Your Honor, the argument that they're now making to you is that they -- because they go to this -- to a common voltage source is the moral equivalent of this: You have a socket in the wall. You plug in your laptop and you plug in a lamp. They're going into this same power supply but two different nodes for two different purposes. Only the plug that's plugging the lamp in is coupling the lamp. Only the plug plugging the laptop is -- right? When you pull the plug out on the lamp, you're not decoupling it from the laptop. You're just decoupling it. And in this particular instance they never identified any embodiment with that yellow first line, the first power supply to line being coupled to the second line of memory cells. So you can't decouple it in and it's therefore indefinite.

01:55 THE COURT: Got it. Once again I've been rescued by Mr. Lee who answered what I was trying to ask you. If you could respond to what he just said, that'd be great.

01:56 MS. WEN: Okay. The first thing I want to say is that it's very common practice in the art that when circuit nodes have the same name, that means they are the same power supply. So VDD, this node, VDD, this node, they're all the same power supply terminal. And when you understand it that way, you then understand that the first power supply line is coupled to the second power supply line through the power supply terminal. And Mr. Lee gave the example of the electrical outlet, but if you have a single power source and you have two different structures coupled to that power source, those structures are coupled together, and that is how a person of ordinary skill in the art would understand it. For example, we submitted an expert declaration. It's I believe the responsive declaration of Dr. Conte. In Paragraph 42 he explains that again both in Figures 2 and 3, and we've been looking at Figure 2, both clearly show that the first power supply line is coupled to the power supply terminal. The second power supply line is also coupled to the power supply terminal, and, therefore, those two power supply lines are coupled together such that when you decouple the second line -- the second power supply line from the power supply terminal, you are decoupling the second power supply line from the first power supply line. I think Mr. Lee

also noted that this coupling should be disregarded because they're being coupled to the power supply terminal for different purposes, but this is a single memory circuit. You have the first line of memory cells and the second line of memory cells both at some point coupled to the power supply terminal through these power supply lines. And in that way they are coupled to each other.

THE COURT: Anything else?

MS. WEN: No.

MR. LEE: Nothing further, Your Honor.

(Conference between the Court and Mr. Yi.)

MS. WEN: Your Honor, could I just make one comment?

THE COURT: Of course.

MS. WEN: We Googled switching circuit as we've been doing. There are thousands of hits on Google, and I think -- it seems to us that the question of whether a switching circuit does actually recite structure is a very important question for you and so we would love the opportunity to submit additional evidence showing that a switching circuit is a well-known structure. A person of ordinary skill in the art would absolutely understand a switching circuit to disclose structure. We would love the opportunity to submit that evidence if it would be helpful to you.

THE COURT: It wouldn't. I'm going to find that the claim is indefinite. If I thought submitting that would help cure my

concern, I would be happy to let you do that. That's -- our concern is more with the way we have interpreted the way the patent works and the way -- the way we've interpreted the way Figure 2 operates and we think that it's indefinite. It's really -- the problem is not with addressing whether or not switching -- a switching circuit would cure that or not.

MS. WEN: Do you have any specific questions about how that circuit works?

THE COURT: No. Fortunately or unfortunately for you, I have someone who can speak engineering really well. And so I'm pretty comfortable and he and I have discussed it a great deal. And so let's move on to the '373 patent, means for providing the operating voltage to the memory.

MR. SLUSARCZYK: Good afternoon, Your Honor. Dominik Slusarczyk for VLSI.

THE COURT: Pleasure to have you here.

MR. SLUSARCZYK: Likewise. Pleasure to be here.

I think we can hopefully breathe a sigh of relief. We've been talking about inductors and transistors all morning and capacitors, I believe. We can now move on to computer systems, which are still complicated, but since we use them every day, hopefully we have a slightly more intuitive understanding of some of these concepts.

So '373 patent. I'll give a very brief overview of the technology and I'm happy to entertain questions as I do that.

02:02 A couple of decades ago, for perspective, computer engineers
02:02 working on processors were typically focused on performance and
02:02 trying to make them faster. The question really was about how
02:02 to get more stuff done in a given period of time. As they got
02:02 faster and more sophisticated and other developments happened,
02:03 which is that they started more and more to operate off of
02:03 batteries, and while power wasn't a concern early on, it was
02:03 really about how fast you make it and it really didn't matter
02:03 because you were usually connected directly to a power plant.
02:03 But we're now operating on batteries and so we've started
02:03 seeing a trade-off. You can either make the processor faster
02:03 or you can make it more power efficient. You can make it
02:03 faster by increasing the frequency of its operation,
02:03 effectively how many operations per second or however you want
02:03 to measure it's performing. And as that goes up, the processor
02:03 also requires more power, which for our purposes today means
02:03 providing it with more voltage. That concept is known as
02:03 dynamic voltage and frequency scaling which means you can scale
02:03 the processor's frequency by giving it more voltage. You can
02:03 decrease the frequency by taking away some of that voltage and
02:03 thereby also saving some power.
02:03 Typically, not always, but typically the processor is
02:04 making determinations about how fast it should operate and
02:04 therefore how much voltage it requires. It does that in part
02:04 by looking at the workload and examining some of the system

parameters like, you know, is someone actually using the computer? Is the screen on? And so on and so forth. A lot of these can be far more sophisticated than the examples that I just gave.

So the processor is usually in charge of selecting that frequency and the associated voltage that's required to run on that frequency. That frequency and voltage determination typically carries over to the rest of the computer system for a number of reasons. One's that it's simpler. Another is that the rest of the system can't really go faster than the processor, and so if it's slowing down, you want the other components to slow down as well and save power.

But memory, which every computer system pretty much has to have, is special. There's certain ranges within which memory in fact can scale and could get faster and get slower at the same time use more or less power, but there is -- there are certain minimum voltages that have to be provided to the memory. If you get below that minimum voltage, your processor maybe can continue operating in theory, but the memory's going to start losing the data that's inside of it.

And so you run into situations sometimes where you want to save data in the memory because you don't want to reboot the whole computer for instance, but you're also perhaps not using the processors. Maybe it's asleep. You don't want to lose your data but you want the processor to be able to scale down

as low as it can down and so a problem develops, which is you need to be able to give the memory the minimum operating voltage but you also want to be able to scale the processor potentially below that minimum operating voltage for the memory.

So this '373 patent is focused on solutions for how do I achieve that in a way that's practical and functional? I'll take a couple of moments to rebut a couple of points made in Intel's tutorial. I don't want to spend --

THE COURT: In what?

MR. SLUSARCZYK: Intel's tutorial.

I don't want to spend too much time on it, but I know the Court said the Court has reviewed the tutorials and there's a couple of I think important distinctions.

Intel says that the first thing you do in practicing this invention is to test the memory to determine its minimum operating voltage. You can test the memory, but if you look at the actual slide on the actual patent, most of the claims don't require testing. So I want to make clear that's not necessarily something that's integral or required by the invention. It's an embodiment.

Likewise, there's some discussion about switching the voltages, but, again, not a single claim actually requires any kind of switch to take place.

And, finally, I think there's an important point here

which is we talked about how the processor makes determinations about how fast it goes and how slow it goes, and it's not always the processor that makes that determination but it is a determination that's made, whereas Intel's tutorial cites that's the issue and says the voltage fluctuates, but this isn't -- you know, it doesn't just fluctuate with the wind, for instance. There's the -- it's a deliberate decision that's made by the system in order to hit a particular performance target.

So means for providing. The full term here is means for providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage. Both parties analyzed this as a Section 112, Paragraph 6 means plus function term, but Intel has proposed that the term is indefinite. Of course I'll cover those arguments as I go along this afternoon, but I will take you through the nuts and bolts of our analysis first which I think will address many of the indefiniteness points that Intel raises in the briefing.

There are actually three structures in the patent that correspond to the recited function. The power supply selector is the first of them. It's also the most complicated. So I'll start with that and get the hard stuff out of the way.

So I'll take it in three pieces. First, the power supply

selector is very clearly disclosed as providing operating voltage to the memory. Here is an excerpt from Column 2 starting at Line 52 of the patent, Plaintiff's Exhibit 3 at Slide 163. And says, memory 18 also includes a power supply selector 21 which receives VDDmem and VDDlogic. These are both voltage values. And provides one of these to memory array 22 as the memory operating voltage. So clearly the power supply selector is providing operating voltage to the memory which is part of the recited function.

It might be useful to look at the figure for just a split second to put those words into -- as some kind of visual representation, and here again we have a power supply selector that is inside of the memory. It's providing voltage to the memory array and it's choosing between VDDmem and VDDlogic at least in this embodiment. I could easily choose between other voltages and other embodiments.

So the next piece of the function is that that operating voltage has to be at a value at least as great as the minimum operating voltage. And, again, that is very clearly explained in the patent. I'm going to read from Column 3, Line -- starting at Line 30 in one embodiment. While VDDlogic remains above a minimum operating voltage required for successful reads of memory array 22, power supply selector 21 selects VDDlogic as the memory operating voltage provided to the memory array such that the memory operating voltage is substantially equal

to VDDlogic. So, in other words, as long as VDDlogic is high enough, that is what we're providing to the memory in this embodiment. But when VDDlogic is scaled to a voltage that is below the minimum memory operating voltage required for reads, power supply selector 21 selects the higher voltage VVDmem during reads cycles to ensure that reads can still be successfully performed. So reads can still be successfully performed means that we are at least as high as the minimum operating voltage required for reads.

And the final piece here is that all this is done in response to the operating values selected by the processor being below the minimum operating voltage. Now, this is one reason why I dwelt on that fluctuates point from the tutorial. It's not just a matter of fluctuating. It's typically the processor that is selecting these frequency and voltage states, and that's clearly disclosed in the patent. In fact, the patent uses this first phrase DVFS here which I introduced earlier as dynamic voltage and frequency scaling.

So a corresponding encoded frequency, and this, by the way, is starting at Column 8, Line 18, quoted on Slide 166. A corresponding encoded frequency and voltage is provided for each of state 0 through state N. And a little bit further down it tells you that those states are provided -- or selected by a processor 16. And a little further down in that column at Line 31 it tells us that the selected voltage state corresponds to

the desired voltage value for VDDlogic. And, again, VDDlogic is what's being provided to the memory at least as long as it's high enough.

Now, this is a good time to tackle this within argument that Intel has made in the briefing. And I'll make a number of points about this. First, Intel argues that Claim 14 expressly provides that the means for providing, the term we're discussing, must be located within the claimed memory. So as an initial matter, the word "within" is not in the claim. I think we made that point in the briefing and for a good reason. We're really talking here about microscopic structures formed in a die and transistors that are part of the same logical block, for example, Figure 1 I believe we were looking at is -- that's a block diagram, right? So transistors that are part of a single block might actually be scattered throughout the die depending on the electrical and other needs of the system. So it doesn't necessarily make a whole great deal of sense to use the word "then." So we'd be then in a situation of discussing where where's within, where's without?

What the claim does say is that the means providing the operating voltage is part of the memory and the exact language is Claim 14 the memory of Claim 9 further comprising. So it's no dispute that the memory comprises the means. I'm not sure it's fair to say that the means must be located within the memory.

02:13 Secondly, even if that requirement were in place, it's -- I would disagree that it doesn't make sense for something to be within something and still be providing voltage to that structure. Car batteries and flashlight batteries are just a couple of examples. Space shuttles, nuclear submarines. There's a whole slew of examples you'd give here. It'll be easier maybe to tackle this argument if we got some further reasoning about why Intel makes this claim, but certainly as a conclusory matter that it doesn't make sense. I don't think that argument really does anything here for Intel. Of course Intel also has patents that claim exactly these structures which I think further undercuts that point.

02:13 I'll talk next about the scalable voltage regulator which is the second of three structures that correspond to this recited function and we'll take it a little bit easier. We discussed earlier that we're providing a minimum operating voltage and we're doing so in response to a state selected by the processor. So the scale of a voltage regulator is provided as an alternate means to make sure that that voltage is high enough, but the thrust of the entire disclosure is that -- the reason we're trying to provide a higher voltage is because the processor is trying to scale the system down below the minimum operating voltage.

02:14 And so, again, DVFS states -- we already looked at this passage at Column 8, Line 18, but the whole purpose of doing

all this is that we are selecting a dynamic voltage and frequency state that may make the memory inoperable. And so the claim -- the patent discloses that if you don't want to use a power supply selector, you can use a scalable voltage regulator. That scalable voltage regulator is going to be supplying a high enough voltage if the processor wants it to go below that, there is circuitry that can prevent that. And so the scalable voltage regulator is the structure that is clearly linked with that recited function, and that's covered on Slide 172.

The third structure is the charge pump. And, again, it's provided as an alternative way to boost the voltage. It's the same mechanism for the processor selecting the states and the entire system determining that the state may be below the minimum operating voltage, and it says at Column 5 starting at Line 54, so in an alternate embodiment VDDlogic may be boosted during reads through the use of a charge pump. And, again, that's in the context of, quote, unquote, when VDDlogic is to fall below the first minimum operating voltage.

Intel's other indefiniteness argument here is that the recited function is supposedly nonsensical. And I think that's a fairly bold claim. Certainly there's nothing nonsensical about the function itself. We can read it and comprehend the grammar. The argument really that Intel has is that the recited function doesn't, in Intel's view, fit with the

structure of the claim. But as an initial matter, Intel hasn't cited any authority that says that the patent has to disclose an embodiment that not only links the recited function with a structure but that also arranges that structure along with all of the other claim elements in exactly the same way as they are arranged in the claim. I'm not aware of any such authority. Intel hasn't cited it. It's sufficient as we've covered that the structure is clearly linked with the recited function, and I think I covered three structures just now that do so.

Moreover, even if it were true that the power supply selector of Claim 9 and then the means that we're covering today in Claim 14 had to be -- are two different things, they can be mapped onto the same single structure that is black letter law from the Federal Circuit.

And unless the Court has any questions, I am finished with the term.

THE COURT: Mr. Lee?

Oh.

MS SOOTER: Good afternoon, Your Honor. If you're ready, I will dive into a brief tutorial.

THE COURT: I can't get any more ready than I am.

(Laughter.)

MS SOOTER: So I'll go through the first few slides fairly quickly because they overlap a little bit with what Mr. Slusarczyk described as well, but I do want to depart a

little bit on some of the details that I think will be useful to understanding the context of the claims.

So as Mr. Slusarczyk said, this is a patent that's about frequency and voltage scaling. So we'll start with that. And he did mention that --

THE COURT: Let me just make sure.

Can you hear her, Kristie?

THE REPORTER: Can you please move back to the microphone?

MS SOOTER: Sure. I'm happy to.

So as we already heard, integrated circuits can contain multiple components. So among those components include processor or memory, and there is typically a voltage supply associated with the integrated circuit that powers those components.

And in addition there is a speed component. One component of an integrated circuit is how quickly it can execute, and that speed component is determined by the frequency, and I do agree that a higher frequency typically requires a higher voltage. And so the faster your chip is running, the more power it's going to consume. So there is a performance versus power trade-off in general with integrated circuits.

And so this patent is directed to some of the concepts surrounding voltage scaling on integrated circuits. And in particular, when an integrated circuit has voltage that is fluctuating, that fluctuating voltage must stay within the

operating limits of the components on the integrated circuit. And in this case you see that there's a minimum operating voltage and a maximum operating voltage, and the voltage supplied to the circuit can fluctuate within that range.

Now, sometimes, and as Mr. Slusarczyk alluded to this, the different components on an integrated circuit can have different operating ranges. So in this example, and this is the example that the patent relies on as well, the minimum operating voltage of the memory is higher than the minimum operating voltage of the processors, and the voltage that's being provided to both must stay within the narrowest operating range of those components. So it's -- the fluctuation then is constrained.

Now, that leads us to the '373 patent, the minimum memory operating voltage technique patent. The patent describes just what we were saying. The memory sometimes has a higher minimum operating voltage than the processor. And so in order to account for that minimum memory operating voltage, you need to know what it is. So the patent does describe that you need to test and see on a chip by chip basis what is that chip's minimum memory operating voltage so that you never drop below that because you don't want to render the memory nonfunctional by dropping too low.

And the patent proposes a particular solution. The patent proposes providing, and we're on Slide 13, the same voltage to

the processor always. The patent describes a first voltage regulator and a second voltage regulator, and in the quote it actually calls the second voltage regulator an alternate supply voltage. The patent describes always providing the first voltage to the processor. And sometimes providing that same first voltage to the memory and in other times providing the second regulated voltage to the memory. In other words, you may have a switch, if you want to call it that, technically the patent calls it a power supply selector that sometimes can provide -- select the first regulated voltage to provide to the memory and under other conditions provide the second regulated voltage to the memory. But the first regulated voltage always goes to the processor.

So what does that do for you? Well, according to the patent, what it allows you to do is provide the same regulated voltage to both the processor and the logic when that first regulated voltage is fluctuating within the range that's acceptable to both components. In other words, the patent provides for when the first regulated voltage is greater than the memory's minimum operating voltage, then you provide that first regulated voltage to both.

And then if that regulated voltage is being provided to the processor falls below what the memory can handle, then you switch over. You flip the power supply selector over from the first regulated voltage to the second regulated voltage. And

so then at that point you'd be providing different voltage supplies to each component, and that keeps them both within their minimum operating range while simultaneously, according to the patent, allowing the processor voltage to drop below what's being provided to the memory.

So all that looks like is you've got slightly different fluctuations. You may have the processor voltage fluctuating as the yellow line shows. It's fluctuating within its wider operating range, whereas the memory is fluctuating when it -- within its narrower operating range by sometimes sharing the processor's voltage and sometimes getting its own voltage to keep it above its own minimum. And that's really the gist of the '373 patent.

So we can move on to the Markman slides. So picking up where we left off, the question here is what is the definition of this means plus function term in dependent Claim 14? And both parties agree that it is a means plus function term and it should be construed according to 35 USC 112, Paragraph 6, and, therefore, you need to define a function and a structure, and as we've already heard, Intel does contend that's indefinite and VLSI identifies a function and a structure which I will address as we go along here.

And I think it's important as we dive into the meaning of those to talk about where Claim 14 fits into the patent. So Claim 9 is an independent claim. Claim 14 is a dependent claim

that depends from Claim 9. And given the problems of Claim 14 that we're about to discuss, we were somewhat surprised that Claim 14 was added to the case and is now being asserted, but the heart of this dispute and the only disputed claims for this entire patent is this dependent Claim 14. Claim 9 is an apparatus claim for an integrated circuit and it requires a memory and it also requires some of these other things we've been talking about, first voltage regulator, a second voltage regulator and a power supply selector that selects between the first and the second voltage regulators to provide one or the other to the memory, and then 14 adds additional limitations to the memory. It says the memory of Claim 9 has to have these additional requirements.

Now, the parties do agree, as I said, that this is a means plus function term, and if it is a means plus function term, we also agree that they have identified the function that is recited in the claim. So we don't quibble with the wording of the function, but we do say that in context when you look at Claims 9 and 14 together, Claim 14 no longer makes sense, and that's what we're going to talk about.

So I think before we dive into why it doesn't make sense, it might make -- looking at the claim, it might make sense to talk about how it got that way because it explains a lot. The inventors didn't purposely draft Claim 14 to look the way it did. What happened was during prosecution the original claim

that then became Claim 9 looked a lot different than it does today. And when Claim -- the original Claim 11 which is now Claim 9 was first drafted, it had very little in it. All it had was memory that uses an operating voltage wherein the memory is characterized as having a minimum operating voltage. So there's memory with minimum operating voltage and a memory location that stores that minimum operating voltage, and then it was a dependent claim, Claim 18 then, which is Claim 14 now, that added this means for providing the operating voltage to the memory. And then as drafted, it had far fewer problems than it does today, but what happened was the original patent owner had to change that original claim to get it through the Patent Office and they had to narrow it dramatically. They had to add four significant limitations to it in order to get that claim.

So one of the things that the original patent owner had to add was this very last limitation, the power supply selector that was not in the original claim. That power supply selector does what we were talking about a moment ago. That power supply selector sometimes supplies the first regulated voltage as the operating voltage when the first operating voltage is at least the minimum operating voltage. So if the first voltage is high enough for the memory, then the first voltage that's already being provided to the processor is going to go both just like we talked about, but if that voltage falls too low,

then a second voltage is going to be provided to the memory. So that's where it says, and supplies the second regulated voltage as the operating voltage when the first voltage is below the minimum operating voltage. So they're two mutually exclusive conditions. The power supply selector is either providing the first or the second regulated voltage to the memory under different conditions that are kind of those two halves makes the whole. It's either providing one or the other depending on the condition.

THE COURT: It wasn't lost on us as we were looking at this that maybe some things happened as the drafting was going on and in these claims that in hindsight wasn't perfect.

MS SOOTER: I think that's right, Your Honor, and, unfortunately, and this is just a dependent claim and one of many asserted claims in this patent and it is one that did get rendered, we think, indefinite as part of that claim drafting process, and, frankly, it's not the first time that we've seen a dependent claim get a little lost in the shuffle or, frankly, messed up in view of some amendments to an independent claim throughout the prosecution of the patent and it's probably not the last time we're going to see it either. But what's happened here is that the original owner of this patent went to add that power supply selector to get this claim through the Patent Office, but what it did was it didn't -- it neglected to amend the dependent claim Claim 14 and so now what you have is

Claim 9 that already has a power supply selector and then Claim 14 that adds a means for providing the same operating voltage to the same memory, and that's problematic.

And as you saw, we did cite to our expert's opinion Dr. Dennis Sylvester from the University of Michigan who agreed that the fact that the claim is requiring two separate sources of voltage to provide the operating voltage to the memory is nonsensical, especially in the context of this patent and Claim 9 and its existing requirements, and here we show a chart which we also have in our briefing which really shows the two requirements side by side. You have Claim 9 that's already providing the operating voltage to the memory, and the thing that's doing that is a power supply selector and it's doing that when the first regulated voltage is below the minimum operating voltage. And extremely similarly, Claim 14 also requires that the operating voltage be provided to the memory, but this time it calls the thing that's providing that a means for providing the operating voltage to the memory, and it's doing it in response to the operating value selected by the processor being below the minimum operating voltage. And we can talk about the differences between those two conditional statements, the when and the in response to, but they're very similar because they're both conditioning the provision of the second operating voltage as the operating voltage of the memory when another voltage falls below the memory's minimum operating

voltage as the claim specifies.

And so that's one problem, and that's frankly enough, we think, to say that this claim is indefinite because it now requires these two somewhat conflicting but overlapping structures to provide the same voltage to the same memory, but also the claim requires in another nonsensical fashion that the thing that's providing the voltage to the memory be in the memory, and while I appreciate the analogies that VLSI is making and they are superficially certainly easy to understand, they're not technically accurate. Obviously your car battery's not providing a voltage to the car or you would shock yourself when you got in. It's providing the voltage to the engine just like when you provide batteries in a flashlight, you're actually providing voltage to the lightbulb, not the flashlight. Otherwise, you would shock yourself when you used it, and that's the same problem -- that analogy is the same problem that we have here with the voltage being in the memory and being provided to the memory at the same time.

So, again, the fact that the function does not make sense within the context of Claim 9 in view of the amendments to Claim 9, that's enough to hold this claim indefinite, but, further, because those aren't logical functions, there's no structure disclosed in this patent that performs those functions. So neither one of the two things that we've just described are actually -- neither two functions we described

are disclosed in the patent first of all. There's no embodiment that has both of those structures providing voltage to the memory. And, second of all, there's no embodiment where there's a component within a memory providing voltage to the memory. And, finally, we don't believe that the structures that VLSI has identified actually even perform the function because no structure is clearly linked to this actual function where the value, operating value is selected by the processor.

So I'll talk about each of those briefly. We already talked a little bit about the fact that you need -- that there's no embodiment that provides two structures. Instead -- that both provide the operating voltage to the memory. Instead, the patent discusses a power supply selector. It never says that there's both a power supply selector as Claim 9 requires and another structure that also provides the voltage to the memory when the first operating voltage falls below a threshold. There simply aren't two structures disclosed in the specification in any configuration that both do that.

Second of all, we have this problem with the memory. Now, I guess the other thing I do want to point out with the problem that there -- with the voltage being inside the memory and being provided to the memory simultaneously, and this is telling. Dr. Sylvester offered an opinion in support of our brief where he -- we talked to him about it of course and vetted this with him and he said that it doesn't make sense

that you would provide a memory -- voltage to the memory and also from the memory, but what I think is very telling is that even though VLSI submitted three expert declarations from Dr. Conte, Dr. Conte never contradicted that. So this is something that is attorney argument about the batteries and the flashlights and the cars, but Dr. Conte never said otherwise, and you would certainly expect that he would have in one of those three declarations.

THE COURT: Why don't you -- I'm going to interrupt you just because I've -- that's an important point. Let me hear from opposing counsel on that specific point and then I'll let you get back up just so I can stay focused on that one because I think that's -- may be to me the key of what I want to do.

MR. SLUSARCZYK: Can I just get some clarity specifically on which point, Your Honor?

THE COURT: The very last point she made with respect to the fact that it was from and generated by both. I'm sorry. It was the power going to and also generated by.

MR. SLUSARCZYK: So the claim talks about -- let's look at the claim language to make sure we're on the same page.

THE COURT: Okay.

MR. SLUSARCZYK: So Claim 14, means for providing the operating voltage to the memory. So we're providing voltage to the memory. I think the analogy's about providing a voltage that had to do with generation like a battery for instance.

The idea here is the battery's providing the voltage to the structure that contains it. It's -- you can argue about whether a battery's actually generating anything or whether it's simply providing energy that was generated at another time, but the point we're trying to make here is that you can provide a voltage to a structure from within the structure, and the claim doesn't have anything to say about where that voltage is coming from. And I think if we read this in light of the specification, it's very clear all of the structures of the integrated circuit are getting their power from off of the integrated circuit. That's simply the way they work. There's no disclosure of any sort of power generation taking place on the integrated circuit, and that would probably be a completely different field of endeavor for this patent.

The providing a voltage can be done by many structures. What the power supply selector and the other structures that we have identified do is they may receive a voltage. That's sort of an antecedent outside the scope of this analysis kind of thing. They are providing the voltage by making the determinations about which voltage is to be provided at what time.

Does that address the point that the Court would like to hear about?

THE COURT: It does. And does the charge pump -- what does the charge pump do with respect to providing higher

voltages to memory?

MR. SLUSARCZYK: I believe that's in Column 5. The charge pump is disclosed in connection with boosting the voltage of VDDlogic when --

THE COURT: So -- I'm sorry. So it only increases it?

MR. SLUSARCZYK: It will -- if VDDlogic falls below the level of the minimum operating voltage, the charge pump, as I understand it, will cause an increase in the voltage to make sure that the memory is still receiving the minimum operating voltage as recited in the function.

THE COURT: And that's the function is to increase -- that's its function in this case?

MR. SLUSARCZYK: Well, it's -- it's providing the voltage. It's not merely increasing it.

THE COURT: I get that, but I'm saying, it's not -- it doesn't operate to decrease it?

MR. SLUSARCZYK: No. No. The charge pump will not decrease the function.

THE COURT: That was my point. Okay. And I'm -- you addressed the point I wanted and I'll let counsel for Intel resume if she had other points. And I appreciate her letting me interrupt her.

MR. SLUSARCZYK: Thank you.

MS SOOTER: So I will say --

THE COURT: And you can certainly respond to what was just

said. That was sort of my reason for interrupting you so you could -- we could focus on this one point.

MS SOOTER: Sure. Well, what I will say is this, just to pick back up on that, you know, from the memory to the memory point is that the patent actually is precise when it talks about providing the voltage to what it's providing it to and it's actually providing it to the memory array. So it's kind of like when I talk about the flashlight having a voltage providing it actually to the lightbulb, not the flashlight itself, when the power supply selector is inside the memory, and I'll just point to it on Slide 16, the memory is 18. When the power supply selector is inside of it, it's providing a voltage to the memory array. So not to the memory.

There is an embodiment, and it says that over and over again in the patent. The citations are on Slide 16. The patent does disclose an embodiment where the power supply selector is outside of the memory and in that -- this is a modified version of Figure 1. It's not actually a figure in the patent, but we depicted it. So we moved what the patent says that it may be outside of the memory. So we moved the power supply selector outside. We can see it's outside of this memory box which was labeled 18, but then it's not in the memory as the claim requires. And so that's Slide 17.

And then to address the charge pump briefly, let me find that slide that I have.

02:40 So as Mr. Slusarczyk mentioned, they do say that the
02:40 charge pump is one of the structures that can be a structure to
02:40 provide the function. We disagree with that. So there are a
02:40 couple of reasons for that. First of all, there's only one
02:40 place in the entire patent where the charge pump is mentioned,
02:40 and that is on Column 5 at Lines 58 to 61. So three total
02:41 lines. And it says, in an alternate embodiment, VDDlogic may
02:41 be boosted during reads through the use of a charge pump where
02:41 this boosted VDDlogic is provided to a memory array 22 for
02:41 reads. So it's just saying this is -- and a charge pump is
02:41 nothing more than a series of capacitors and switches that
02:41 store energy and then let it go when you want to boost a
02:41 charge, boost voltage, and you can let it go. And what it's
02:41 saying -- to boost the voltage. And what it's saying here is
02:41 that if you wanted to use a charge pump, you can use it to
02:41 boost the voltage during reads, but that's not the function
02:41 that we need to find the structure for. So it's not a
02:41 structure that's clearly linked to the claimed function that we
02:41 both agree on. The function is above. The function that we
02:41 agree on is providing the operating voltage to the memory at a
02:41 value at least as great as the minimum operating voltage in
02:41 response to the operating voltage selected by the processor
02:42 being below the minimum operating voltage. So in order to be a
02:42 structure here, it needs to be tied to that conditional check.
02:42 Did the voltage that was requested by the processor fall below

my threshold? If it did, I'm going to switch over or boost the voltage or whatever, but that's not what the charge pump in the patent is doing.

There is one other structure that's on Column 8, and it is the scalable voltage regulator. And this one's a little bit complicated, but what they're doing is they're pointing to No. 24 as a scalable voltage regulator and saying that that's a structure that can provide the function in the claim.

And, Mr. Lee, if we could go to Claim 9 and if you could bring up Claim 1 side by side.

So remember what we're talking about here is VLSI says that the means plus function element within Claim 14 can be No. 24 -- according to the patent can be No. 24, Item 24. So we're going to look at --

Actually Figure 1. Sorry.

We're going to look at what 24 in Figure 1 is. So 24 is actually this voltage regulator, the one that's always provided to the processor. That's the first regulated voltage. It's already being provided so that --

If you can scale back out again.

It's always being provided to the processor, but sometimes -- and that's what Claim 9 says, a first voltage regulator for supplying a first regulated voltage, and that's what's being provided to the functional circuit. And the second voltage regulator is 26, and that's sometimes provided

to the power supply selector and other times the voltage -- the first voltage from the first voltage regulator as being provided.

So even though Claim 1 is pointing to these two as the first and the second, now VLSI is trying to argue that the second voltage -- the first voltage regulator can also be the first voltage regulator and it just doesn't make sense when you look at the fact that what they're pointing to is actually the opposite of what the claim would require. So we believe I guess for all of those reasons that, first of all, given the amendments to the claim during prosecution, the function no longer makes sense, and because the function doesn't make sense, there are no structures that perform that function disclose, and for each of those separate reasons, the claim is indefinite, but even if there were the -- of the three structures that VLSI has identified, the first is essentially just pointing to what Claim 9 already requires. So that's by default presumptively the wrong interpretation, because --

If you could go to Slide 24.

The law tells us that the separate naming of two structures in a claim strongly implies that the named entities are not one in the same structure. So their first structure is presumptively incorrect.

The second structure, the charge pump, doesn't perform the right function as disclosed in the patent.

And the third actually contradicts its independent claim Claim 9.

THE COURT: Okay. Anything else from VLSI?

MR. SLUSARCZYK: Briefly. Just to --

THE COURT: Give me one second.

(Conference between the Court and Mr. Yi.)

THE COURT: Go ahead, please. Thank you.

MR. SLUSARCZYK: First to respond to the discussion of the amendment history of the claims. It's pure speculation. Absolutely no evidence has been offered. Counsel used terms like messed up, neglected to amend, even made the claim that the inventors didn't intend for the claim to use the words that it does today. There's zero evidence for any of this. The U.S. Patent Office approved the claim and issued it and the claim should be respected as it appears in the patent document.

Next counsel argued that two separate structures can't provide a voltage to a memory, but as far as I can tell, the only support for that, if it supports it, is the expert declaration. In fact, the charge pump example that we were discussing, it could be viewed as two separate voltage sources providing voltage to the memory because it's both VDDlogic being provided by a voltage regulator as well as a charge pump providing voltage.

THE COURT: Where's the charge pump located?

MR. SLUSARCZYK: I think one having ordinary skill in the

art could locate the charge pump in different locations. I think the requirement would be that the charge pump has to be coupled to the conductor that's bringing the VDDlogic to the memory, but it certainly could be part of the memory component, whatever -- wherever we would draw at that particular boundary.

THE COURT: So you're going to have to rely on your experts to find a charge pump in the Intel products? Is there going to be a dispute over what the charge pump is between the experts?

MR. SLUSARCZYK: I'm not sure that we're pointing to a charge pump at the moment. And so that's unfortunately --

THE COURT: Well, you guys want me to include charge pump as one of the structures, right?

MR. SLUSARCZYK: That's because the patent discloses it. So we're going for correctness. We're not simply including those things that are convenient and then leaving out the others.

THE COURT: Okay.

MR. SLUSARCZYK: Finally -- or perhaps not finally, but getting to the end here, counsel argued that the power supply selector of Claim 9 and the means of Claim 14 are, quote, unquote, somewhat conflicting, but no conflict has actually been identified, and in fact --

THE COURT: Let me -- have you -- has Intel heard anything they want to respond to so far?

02:48 MS SOOTER: The one thing I would just state, Your Honor, at the risk of saying something that I know you already know, is that is that the means plus function case law it does require that the structure be clearly linked to the claimed function, and the charge pump clearly is not, and you can't impute structure to the charge pump or a location to the charge pump based on the ordinary skill in the art. It has to be disclosed in the specification.

02:49 THE COURT: Okay. Josh?

02:49 MR. SLUSARCZYK: I would like to respond to that, but I can wait.

01:58 (Conference between the Court and Mr. Yi.)

02:49 THE COURT: I'm going to go ahead and I'm going to find that the claim is not indefinite. We're -- I'm going to construe the structure as being a power supply selector and only a power supply selector.

01:58 (Conference between the Court and Mr. Yi.)

02:49 THE COURT: I'm sorry. And equivalence thereof or equivalence thereof.

02:49 MR. SLUSARCZYK: Could I please briefly respond to the point about the charge pump? I think they're fairly important.

02:50 THE COURT: It's not going to change my mind.

02:50 MR. SLUSARCZYK: Okay. So with the Court's permission, I'll move on to '983 patent.

02:50 THE COURT: That'd be great.

02:50 (Brief off-the-record discussion.)
02:50 THE COURT: Actually, I'm being told we're going to take a break. And so -- by higher powers. So why don't we resume -- how many claim terms do we have left? Three? Four?
02:50 MR. SLUSARCZYK: Four.
02:50 THE COURT: Four? I think we're doing great. And so why don't we take a little bit of a long break and go 20 -- to have a 20-minute break until 3:10 and then we will -- we'll finish up with the remaining claim terms.
02:50 THE BAILIFF: All rise.
02:50 (A break was taken from 2:50 to 3:17.)
03:17 THE BAILIFF: All rise.
03:17 THE COURT: Thank you. You may be seated.
03:17 Who's next?
03:17 MR. SLUSARCZYK: I'll take a few minutes to introduce the '983 patent.
03:17 THE COURT: Okay. And I didn't mean to be impolite to you earlier by not having you argue that, but we'd -- I think we already pretty well decided that wasn't something we were going to include and so I don't think it would be a good use of our time for you to make that argument. So...
03:17 MR. SLUSARCZYK: And we have limited time and plenty to get through.
03:17 THE COURT: Well, we don't -- really we have unlimited time for you guys. It's just I'm skeptical it would change my

mind.

MR. SLUSARCZYK: Appreciate that. Thank you.

So the '983 patent, the title is sequential ordering of transactions in digital systems with multiple requestors, and I promise when I finish my tutorial in a few minutes, that will make sense.

Computer systems typically have a processor and we've discussed that already in context with the last patent. They also usually have a number of peripherals like keyboards, audio controllers, display controllers and so forth. And I've colored those here in blue in Figure 4 of a patent which shows one of the exemplary embodiments.

We don't usually think of the processor and the peripheral as peers. They perform -- generally we think of them as doing different things, but for purposes of this patent, they are all peers in the sense that all of these devices operate on data. They do work with data. So the processor will perform computations of all sorts. And the peripherals will do things with the data. So just displayed on your computer screen or in the case of the audio controller, you have a microphone, for instance, that is an analog input signal as being transmitted into ones in -- transformed into ones and zeros and out of the speaker it's the opposite where a string of ones and zeros is being transmitted or transformed into an analog audio signal.

The digital data, the ones in the zeros, are typically

stored in memory or in some other resource, and that other resource can be on the computer. It could be a disk drive. I won't focus on that for the remainder of my presentation because typically the component of most concern that actually holds the data is the system memory.

And, now, because of the way computers are structured, typically these peripherals and the memory are in different parts of the system. They may be situated inches from one another or even closer, but in terms of everything that is between them in that computer sense, there's quite a bit going on. And so for -- in order for these peripherals and the processor to access the data and the memory, the computer provides something called a bus system. Here it's labeled Bus 310 or network of Buses 310. The analogy only gets you so far, but for purposes of this tutorial, we can actually think of the bus system as an actual bus as something that shuttles things back and forth.

THE COURT: I actually had a bunch of cases. I -- on this stuff. I'm pretty familiar with this technology.

MR. SLUSARCZYK: Excellent.

And so the specific thing that's being transmitted across the bus here is requests and responses. The requests typically come from the processor and the peripherals, and there are things like read or write to memory. That's why they're called the requestors in this context.

The other thing that travels over typically is the responses from the memory. And so if you have a read request, the response will typically contain the data that has been read.

So going back to the title sequential ordering of transactions in digital systems with multiple requestors, the final piece is the sequential ordering piece. When you have a lot of data traveling over the bus system because you have a number of peripherals, for instance, the order in which the requests and the responses are processed and the order in which they are sent can make a difference. The classic example we usually give is if you have a write followed by a read, you expect that read to give back to you what you just wrote. If those requests were processed in reverse order, you might have unexpected behavior because you'll read back something that you -- something other than what you just wrote, and that could lead to all sorts of buggy behavior.

As I did with the previous patent, I'll respond very quickly to a couple of points in Intel's tutorial. The first is Intel's slide -- I believe -- it looks like it's Slide 14. It makes the claim that the patent proposes allowing the requestors to dictate the order in which the access requests are performed, and that's not exactly correct. The claim says that the requestors provide an indication of an order. That's a little bit different than dictating the actual order.

Likewise, that order, although Intel says that you have the requestors dictate the order rather than the policies implemented in the bus network, but the order indicated in the embodiments can at least in part be implemented by reference to policies from the bus network. For instance, here we have a quote from the patent talking about some embodiments. In some embodiments it says, multiple requests having the same thread ID value may be performed in any order as long as they are performed subsequent to transactions having a lower or higher thread ID value. And so that thread ID value in this embodiment gives you an indication of an order, but it does say that in some circumstances they can be performed in any order, and in that situation the bus can easily apply its own policies to figure out what the best order can be.

So the term we're looking at today is an indication of a/the specified order and it appears in every independent claim of the '983 patent.

I've highlighted in Claim 1 but we're going to be looking at it in context, and it starts up here with the wherein clause. It's, wherein each access request includes an indication of whether or not this occurrence of the access request is to be performed in a sequential order among other occurrences of the request, and, if so, an indication of a specified order.

VLSI's proposal here is plain and ordinary meaning, and

I'll explain a little bit how we arrived at that proposal in the coming minutes. Intel's proposal is that this should be construed as a second, different indication that indicates a/the specified order. And so I'll focus on some of the problems that we perceive with Intel's proposal.

As an initial matter, Intel is unclear about whether it's proposing something with a different scope than what the plain and ordinary meaning language is or not. Intel certainly claims that the plain claim language supports Intel's construction, and you would think from reading the briefing that Intel is simply attempting to offer what it thinks is a better version of that plain claim language. And, in fact, it's providing that claim language. Here I've created a table to sort of show what the -- what the difference is between Intel's proposal and the actual claim term. And I think a salient -- part of this analysis is that Intel isn't clarifying any technical words. They don't appear to be contending that there are any terms of art that need definition. For example, the word "indication," which could arguably be seen as a technical term, is simply repeated in Intel's construction as is the specified order. What Intel has done here is reordered some of the orders, perhaps rewritten a few of them and added the phrase "second, different."

We already saw I think this quote earlier today, and when you have a situation like this where the parties aren't really

disputing the plain meaning, it certainly seems like Intel isn't proposing to clarify or change anything other than adding these words which I'll get to in a minute. It seems to support a plain and ordinary construction of the term.

What we do take issue with is the changes that Intel is proposing to make to the claim term. First of all, they're adding this second, different language, and, second of all, they're crossing out of and turning that into that indicates, and both of these changes potentially alter the meaning of the claim. And we haven't heard from Intel what the import of those changes would actually be.

So one indicator here -- and excuse the pun -- is one indicator that Intel's construction is incorrect here is it cuts out a large number of embodiments. So I'll cover one example here which is the patent talks about embodiments where a transaction ordering signals are the mechanism through which you provide the claimed indication. And it tells you -- and this is Column 6 starting at Line 35 -- that any one or any two of those transaction ordering signals can be omitted. And in particular there's three of these different signals. There's the thread ID signals, number one. There's a sequence number signals, number two, and the last-in-thread signal, number three. So effectively the patent says you can have all three, but you can also have all one and that's still an embodiment of the invention.

So we'll focus on the one where we are just looking at -- focus on embodiment where two are omitted. So we only have one mechanism for providing the claimed indication. And it says, if sequence No. Signal 372 is the only transaction ordering signal used, then a value of zero is used to indicate an unordered transaction and requests with non zero sequence numbers are performed subsequent to transactions having a sequence number that is lower in value.

So it's a very simple example of how we can use one mechanism to provide the indications that are recited in the claim, right? And it's -- this is an optimization that engineers make all the time. You can use a zero value to indicate that something's not present, and if it's non zero, that further information, whatever the value is gives you some quantity that is then useful, given that something is present.

Now, Intel hasn't told us what second or different in its proposed construction actually means, but it certainly seems like Intel is trying to cut these embodiments out of the scope of the claims because it isn't clear whether if you have one mechanism that's providing an indication of whether ordering is present then providing an indication of the actual ordering -- I'm paraphrasing the claim here. Is that a second and different indication? Intel has not answered that question.

Intel looks to the prosecution history in order to justify the language. As an initial matter, I'll throw out a

proposition that I don't think is controversial which is we can't just go into the prosecution history and pull out any word and stick it into the claims under the guise of the applicant said it and therefore it should be appended to the claim. That of course is not how this process works.

Intel makes the argument that the applicant in distinguishing a prior art reference called Weber made an argument that Weber didn't correspond to the claim language that was pending at the time because Weber didn't have two different indications. Well, of course these statements have to be right in context and we can't just throw out the Weber reference and pretend like the second and different language was meant as an all purpose redefinition of the claim.

When we look into what actually was argued, the examiner for most of the prosecution period was unclear as to what in Weber actually corresponded allegedly to the claimed indication term. And so the applicant's, in trying to get further clarity, repeatedly said, you have to look at all of the claim language. It says indication twice. You've only accounted for one of them.

In arguing that there's a second and different indication, the applicant was just talking about the claim language as an object. They weren't trying to redefine the scope of the term. They certainly weren't commenting on the meaning of any given indication. They were just saying, look, examiner. Can you

please give us your theory?

Finally, on appeal the examiner clarified. As it turns out that what -- the thing in Weber the examiner was pointing to was a single bit, and so the applicant said, look. However you -- however you slice this, there's a single bit. It can't give you more than a single piece of information by definition. It's a zero or a one. And so that might tell you whether ordering is present, but it certainly doesn't tell you what the ordering is because once you've accounted for is there an ordering or not and you've exhausted the informational content of that bit.

The single bit example of Weber, this is -- you know, it's a rain drop in the ocean. Intel is taking this language and attempting to drain the entire ocean with it by saying that the applicant made a statement that completely redefined the scope of the claim. Certainly there's nothing in the prosecution history --

THE COURT: That was a great line.

MR. SLUSARCZYK: Thank you.

THE COURT: Who wrote that line?

MR. SLUSARCZYK: I wrote it as I was scribbling on my notes today.

THE COURT: That was just a great line.

MR. SLUSARCZYK: I hope it made my point.

THE COURT: A little hyperbolic but great.

MR. SLUSARCZYK: I hope it made my point. I think hyperbole is slightly in order because there's such a disparity between what was actually said and the meaning that's being ascribed to it and the argument.

Black letter law says that a disclaimer of the sort that Intel is seeking here has to be clear and unambiguous. If there's ambiguity whatsoever, you do not find disclaimer on this record with extremely limited statements that were made by the applicant. It would simply be an inappropriate thing to take the words "second" and "different" and splice them into the claim without consideration of the completely different context in which those words might be applied in the future.

If the Court has no questions, --

THE COURT: I don't.

MR. SLUSARCZYK: -- that concludes my presentation. Thank you.

THE COURT: I have great anticipation that your rebuttal -- you have to have another great line.

(Laughter.)

MR. MUELLER: I'll work on it, Your Honor. Thank you.

Your Honor, I think I can dispose of the tech tutorial and move right to the Markman issues.

THE COURT: You can.

MR. MUELLER: Thank you.

So, Mr. Lee, if you can pull up the Markman slides.

03:32 The first is the title of the patent is important, and I'm going to come back to the exact reason why, but, Your Honor, as you heard, it's sequential ordering of transactions in digital systems with multiple requestors. And different techniques for accomplishing that goal, the sequential ordering of transactions in digital systems with multiple requestors.

03:32 And the term at issue is an indication of the specified order. And, Your Honor, our argument for this claim term has two prongs, but at bottom amounts to the plain meaning of the claim terms. Now, we do think the prosecution history confirms that plain meaning, but we think the language of the claim itself is dispositive as well, and if I may approach the screen, Your Honor.

03:33 We have here in the third limitation down, wherein each access request includes -- and here's the first indication -- an indication of whether or not this occurrence of the access request is to be performed in a sequential order. So the first indication that's recited in the claim is whether there will be ordering at all. And if there were -- if the answer is no, that's the end of the analysis for purposes of sequential order. If there's no ordering by definition, there will be no sequential ordering.

03:33 Then the claim continues. It says, whether or not this occurrence of the access request is to be performed in a sequential order among other occurrences of the access request

and, if so, an indication of a specified order, and that's the second indication. So if the first one is present, if there's to be an ordering, then we look to the second indication to see what the order should be. So the claim itself recites two different indications. Not just one. It recites two different indications. And we know that in part because of the conditionality. The second indication is contingent on the first. If there's no ordering at all, there will not be a second indication. If there is ordering, then there will be a second indication, and the second indication will give us the specified order. So that's what the claim says.

Same is true in Claim 11. It's a little bit different wording but the same concept. It first recites an indication of whether or not this occurrence of the access request has a specified order. That's the threshold indication. And then it goes on to recite, in a separate limitation, an indication of the specified order in those occurrences of the access requests that are ordered. So again we have conditionality. We have two indications where the second one is contingent upon the first.

And our construction is just that, that the second indication -- so the second instance in which the word "indication" is used -- refers to a second different indication of the specified order. We don't use the word "dictate." We say a second different indication of the specified order, and

that is the plain and ordinary meaning if you -- given the language of the claim, the grammar of the claim, the disclosure in the specification and the prosecution history, and plain meaning is to be judged by a person of ordinary skill reading all of that intrinsic evidence, and reading all that intrinsic evidence, that is what the plain and ordinary meaning is. The second indication recited in these claims is a second indication different from the first, conditional on the first contingent on the first but different than the first.

And so that's the dispute, Your Honor. The dispute is whether the claims require two different indications or a single indication. The claim language, as I just walked through, we believe confirms our construction. Each independent claim requires two separate and distinct indications in the access request, each of which must include different information. The first one is the threshold indication which indicates whether or not we have ordering. And the second is if you have ordering, the specific order. Two different indications.

And the statements during prosecution, Your Honor, also confirm this construction. I'm now at Slide 5 and this is a quote from an appeal brief that the applicants filed after the claims were finally rejected by the examiner. And they stated in that brief that appellant's claimed invention includes two different indications, each of which are provided by the access

request. A first indication is related to whether the access request is to be performed in a sequential order among other occurrences of the access request. A second indication is used conditionally relative to the first indication and is related to an indication of a specified order.

Now, that's exactly what I just said, Your Honor, that there's two different indications. The first one is conditional on -- the second one's conditional on the first, but they're two different ones, and our construction reflects exactly what they said to the Patent Office. Your Honor, they could have said, we are claiming one thing that serves two different purposes. That's not what they said. They said the invention is two different indications, each of which are provided by the access request and then distinguished among those two and made clear how one is conditional on the other.

Now, they also said the Weber reference does not teach that access request contain these two different indications. The examiner has not provided any specific indication as to what is, went on to explain they did disagree with the examiner's conclusion as to whether those two different indications were met. But they were distinguishing the Weber reference -- I'm going to be coming back to the Weber reference in a bit -- on the basis that it lacked the two different indications and that the claims required those two different indications.

Now, you did hear that there's multiple embodiments in the specification, and that's true. There are multiple embodiments in the specification, but with respect to this term "indications" and how the claims were actually drafted, the plain meaning of those claims and how they were explained to the patent examiner, what they claimed is two different indications. There are embodiments in the patent that have exactly that, and in particular there are embodiments that use a thread signal and a sequence number. Those are labeled I think with the 370 and 372 in the specification as two different things that serve those two different functions. The thread signal served to indicate whether ordering would be present at all, and the sequence number indicated the specific ordering where there was an order. So there is a claimed embodiment covered by these claims, Your Honor.

THE COURT: Well, then let's turn to Paragraph -- I'm sorry -- Column 6, Line 64 if you can.

MR. MUELLER: Sure.

Mr. Lee, can you bring that up, please?

THE COURT: And that reads, if sequence number signal 372, which you were just discussing, is the only transaction ordering signal used, then a value of zero is used -- there's probably a word "to" that was left out -- to indicate an unordered transaction. Requests with non zero sequence numbers are performed subsequent to transactions having a sequence

03:39 number that is lower in value.

03:39 So doesn't that -- how does that square with what you just

03:40 said?

03:40 MR. MUELLER: That is an embodiment, Your Honor, and as I

03:40 said, there are multiple embodiments. That embodiment is not

03:40 claimed. It's in the specification, to be sure. That is a

03:40 signal data -- signal piece of information as opposed to

03:40 multiple, but that's not what they claimed. So it is

03:40 absolutely their case that that's in the patent. It's not

03:40 covered by the claims under the plain meaning or as illuminated

03:40 during their discussion with the examiner.

03:40 And if I go back to the deck -- unless Your Honor has

03:40 further questions on that.

03:40 THE COURT: I'm going to ask VLSI to respond to that

03:40 argument, but nothing else for you.

03:40 MR. MUELLER: Sure. So the applicant's repeated assertion

03:40 during prosecution that the claims require two different

03:40 indications is directly relevant to the plain meaning. So I --

03:40 we're not here to argue, Your Honor, that there's a superficial

03:40 meaning of the claim that would be broader and they have

03:40 disclaimed for this particular term. The plain meaning is

03:40 identical to what they explained to the examiner. So both as a

03:41 matter of the grammar of the claim but also the plain meaning,

03:41 when understood in light of the full intrinsic record,

03:41 including the back and forth with the examiner, it's the same.

03:41 And if there -- if there were a broader meaning, it would
03:41 operate as a disclaimer, but again we think the meaning in the
03:41 plain -- the meaning in the grammar of the claims itself is
03:41 plain and consistent with our position.
03:41 So if we could go to VLSI's argument. This is the single
03:41 drop of water in the ocean argument, I believe, Your Honor.
03:41 And I want to show you if I could that we're not trying to
03:41 drain the ocean. We're trying to swim in it, whatever is the
03:41 right term to give full respect to what is there. We want to
03:41 show you exactly what they said and what they were arguing
03:41 against at the time of the prosecution.
03:41 So let's pull up the Weber reference itself. And
03:42 remember, if we could, the title of this patent talks about
03:42 sequential ordering. Okay. So sequential ordering. And the
03:42 question on the table is, do they need one indication or more
03:42 than one indication within the meaning of the claims? Can the
03:42 claims be met and should the claims be construed to embrace a
03:42 single indication or do they need more than one indication as
03:42 claimed?
03:42 And, Your Honor, this is the Weber reference. This is
03:42 what was at stake before the examiner and on appeal. It's a
03:42 U.S. patent and it's titled various methods and apparatuses for
03:42 arbitration among blocks of functionality. And it also deals
03:42 with arbitrating among multiple respects -- requests for access
03:42 to common resources.

And, Mr. Lee, if we could go to Figure 8, please.

Your Honor, this is Figure 8, and these various branches are branches that are containing flows of requests from different processors seeking access to common resources. So we have Branch 0, Branch 1 and Branch 2 and then various requests being made over time. The question is, how do you sequence among those requests and create order among them? And I think what you heard is that what was at issue in the Weber reference was a bit that might tell you at most whether there was ordering but not what the order would be. Not the actual order itself. So that was the argument that was put to Your Honor, I believe. And I want to test that by looking at the actual language of Weber, and if we go to Column 8, Lines 13 to 27.

So this is Figure -- a description in the text of Figure 8, Your Honor. The figure we just looked at. And this states: Figure 8 illustrates the same transactions from the first Branch 802 which includes Transaction A0, A1 and A2 from the second Branch 804 Transactions B0 and B1 and from the third Branch 808 transactions C0 and C1. So just a pause there. This is in text terms describing three streams of transaction requests for these common resources. Then it continues: And the same first global group of transactions 836 is formed, however. The sequential order of how the shared resources sequentially processes and receives these transactions to service these transactions has been altered. So we already

have a cue here that we're talking about the exact same thing as the '983 patent. It uses the term "sequential order," the same term found in the title of the '983 patent.

Then it continues: The field configurable component upstream of the arbitration controller has attached a locking indication 844, locking indication. So we don't have to guess at whether this patent was teaching us an indication of a specified order. It actually tells us it uses the term "indication," singular. Singular indication.

And then it goes on to say: On Transactions A0 and A1 to ensure that the shared resource services, these indicated transactions sequentially. Thus, the order within the first group of transactions 836 to be serviced starts off with A0 and then is followed by A1 and then sequentially B0 and lastly C0.

So the indication that was at issue in that patent taught on its face a sequential order. It doesn't just say whether there should be ordering. It teaches us precisely what the sequence should be and enumerates it in this paragraph.

So this is the drop of water, Your Honor. The patent itself uses the term "indication." It teaches using an indication to arrive at a sequential order. So it teaches both ordering and the sequence in which that order should take place. It is far from a drop of water. It is a very fulsome statement as to what would happen in the Weber reference.

And in reaction to that Weber reference to overcome that

Weber reference, if we could go back to Slide 11, Mr. Lee, what they said in their appeal of the examiner's decision is, the examiner's analysis is improper as it conveniently ignores the claim language supporting the second indication. The claim language immediately following the examiner's selected expert is, and if so, an indication of a specified order. Thus, the claim language explicitly recites a first indication of whether to perform in a sequential order and a second indication of the specified order. The examiner's interpretation improperly ignores claim limitations directed towards two different indications.

So what we have in front of us, Your Honor, this is the record. The Weber reference when we actually look at it and actually examine the text of the specification, the figures that were being described on its face use the term "indication" and taught how that indication would be used not only, not only to indicate whether there was ordering but how to have the sequential order set, what the precise elements would be and what order they would be transacted.

And against or in the face of that prior art, what they told the Patent Office is, no. We're different. Our claim limitations are directed towards two different indications. And that, Your Honor, is exactly what we're asking for Your Honor to construe the claim to mean.

Mr. Lee, if you could return to the claim construction.

Next slide, Mr. Lee. I'm sorry.

All we are asking, Your Honor, is that they be held to precisely what the plain meaning is, precisely what they told the Patent Office in the face of the Weber reference. The second indication is a second different indication.

Thank you, Your Honor.

MR. SLUSARCZYK: So I'll respond to a number of points that Mr. Mueller made. First, it sounds like Intel's not making a disclaimer argument. What I heard from Mr. Mueller is that Intel is arguing that its proposed construction is simply the plain and ordinary meaning and they're going to the prosecution history in order to, quote, unquote, confirm that plain and ordinary meaning.

THE COURT: That's the way I heard it.

MR. SLUSARCZYK: Thank you.

The plain and ordinary meaning that they're proposing violates black letter law which very clearly says that the use of two terms in a claim term requires that they connote different meanings, not that they necessarily refer to two different structures. There's no dispute about what the claim language that actually appears in the patent says. It uses the word "indication" twice and it ascribes different functions to those indications. We don't dispute that.

What concerns us about Intel's proposed construction is that the use of the word "second" and "different" seem to put

this black letter law to bed and avoids its application to this -- these particular claims. That's improper. No reason has been given for why that should be done.

Next Mr. Mueller brought up a number of excerpts from Weber and a number of excerpts from the prosecution history to the extent that Intel is in fact relying on the prosecution history to narrow the scope of the claims. And I think what matters for the analysis is the arguments that were actually made by the applicant and the positions that were actually taken by the examiner. There's no dispute that the examiner pointed to a single bit in Weber. In fact, I'm going to read from Page 21 of Intel's opening brief which is DI82, and Intel states: During prosecution, the examiner repeatedly rejected the claims as anticipated by a patent (Weber) disclosing a single bit that the examiner initially treated as satisfying both claimed indications.

Again, the applicant's statements about a second and different indication were simply meant to orient the examiner and later the appeals panel to the actual claim language because it appeared that the examiner was disregarding at least half of it.

To the extent Mr. Mueller was relying on portions of Weber to inform how the claim term should be read, that seems more like a prior art Section 103 and 102 argument that Intel will have an opportunity to make in the future, but for the record

I'll note that the Federal Circuit panel -- or excuse me -- the Board of Patent Appeals and Interferences Panel that reviewed the appeal from the examiner ultimately found that Weber didn't disclose any of the recited indications.

Thank you.

MR. MUELLER: May I briefly, Your Honor?

THE COURT: Sure.

MR. MUELLER: So first, Your Honor, we did say that it was a single bit at issue in Weber. That's -- nothing I said is inconsistent with that. That single bit was being used in Weber to perform these functions, and the way they overcame the Weber reference is to say, we're different. We have claimed this in a way that has two different indications.

And if we could, Mr. Lee, go up to Slide 11 one more time.

Again, this is what they said. They said two different indications. The claim limitations are directed towards two different indications. So there's no doubt that Weber taught an indication. It used that term. There's no doubt that it taught indication for specified ordering. I don't think you heard any different just now. The distinction they drew, as I said, well, we're different. We use these two different indications, not a singular indication, and our position now is they should be held to exactly what they said is consistent with the plain meaning.

And the final thing I'll say, Your Honor, is it's true we

are not arguing the disclaimer. We don't think it's necessary. If Your Honor thought the broader -- the plain meaning was broader, we believe this prosecution history is sufficient to support a disclaimer, but there's no reason to go there. On its face, given the way it's drafted and given the way it was argued to the Patent Office, the meaning is plain. And if our position, the Intel position violates the canons of construction, well, we're just saying what they said. Precisely what they said to the Patent Office what the plain meaning is. It means two different indications, and that's all we're saying.

Thank you, Your Honor.

MR. SLUSARCZYK: Two final points. In explaining the prosecution history, Mr. Mueller put up lengthy paragraphs and dove into a lengthy discussion of the Weber reference. He's providing context for what second and different meant when the applicant said them. The problem with putting those words into the construction is a jury, for instance, applying that construction will not have any of that context, and the words "second" or "different" could mean very different things that were never intended by the applicant. Certainly never intended by the examiner in allowing the claims.

And then briefly I wanted to respond to an earlier point about the embodiments. Mr. Mueller said that the patent spends multiple columns talking about embodiments that aren't claimed,

and that stretches credulity I think. It's very clear the patent is discussing embodiments with one, two or three different mechanisms for providing an indication, and all of those embodiments, including the ones that use a single mechanism, fall within the scope of the claims. Otherwise they would be distinguished in the specification.

Thank you, Your Honor.

MR. MUELLER: And just very briefly on that, Your Honor, there is no canon of construction that claims or presume to cover every embodiment in a patent specification. That is not an accepted canon of construction. There is a presumption that if an interpretation excludes all embodiments, that can be disfavored. That is not what we're arguing. Our position which is the plain meaning of the claim and precisely the meaning they argued at the Patent Office would cover a disclosed embodiment, namely, the thread signal sequence number embodiment. That is perfectly consistent with the accepted canons of construction and there is no canon that requires the claims to require every -- to cover every embodiment.

MR. SLUSARCZYK: Again, I think it's discredulous to say that the applicants would have drafted and disclosed embodiments that aren't covered by the claims, and black letter law says that. The construction that excludes embodiments is presumptively incorrect.

THE COURT: Thank you.

03:54 MR. MUELLER: It doesn't say that, but I've said my piece, Your Honor. Thank you.

03:55 (Conference between the Court and Mr. Yi.)

03:55 THE COURT: With respect to the claim term an indication of a/the specified order, the Court is going to find that the proper construction is plain and ordinary meaning.

03:55 For the remaining claim terms, to speed things up a little bit, though we have all the time we need, it's just -- I think it would be more efficient for the Intel folks to go first since the plaintiff's taking the position on the remaining claim terms of plain and ordinary meaning, correct?

03:55 So I'd like for the Intel folks to go first and then the plaintiff can respond. If I'm correct, the next claim term up is on the '025 patent and it is priority level information associated, et cetera, correct?

03:56 MS SOOTER: Yes, Your Honor.

03:56 THE COURT: Very good.

03:56 MS SOOTER: And I think that the next two terms are broken out on the joint claim construction statement. They both start with priority level information, associated, and both of those we were planning to argue together.

03:56 THE COURT: I would be so very happy if you would.

03:56 (Laughter.)

03:56 MS SOOTER: Okay.

03:56 THE COURT: And I'm -- are there three claim terms left?

MS SOOTER: Yes, Your Honor.

THE COURT: I want you to know how difficult it's been for me to sit waiting the entire day to hear from Steve Ravel, saving the best for last, but that's probably the way I would have done it too just as -- you know, you don't -- whenever they tease you on the shows about some big huge story that you don't -- you have to wait through the whole show to see the last one, it would -- it's a great way to end the day to get hear from Mr. Ravel and others, but I certainly am enjoying -- not to slight you in any way. I have very much enjoyed your presentation here today as well.

MS SOOTER: Well, we will try to get you to the grand finale as quickly as possible.

So let's see. Well, we'll talk a little bit about the '025 patent, and the '025 patent has to do with interrupts. And so I -- this is the patent that Mr. Yi reached out about yesterday and so I thought it would be helpful to provide the technology tutorial here, but I do invite questions obviously. We want to make sure that we cover what would be helpful to the Court, and if we don't, we would very much like to hear how we can help.

Just talking about interrupts.

THE COURT: I'll let you know again I handled several case -- I'm pretty familiar with this concept.

MS SOOTER: Oh, good.

THE COURT: And so you can go pretty quickly through the tutorial. Say whatever you'd like, but I actually understand the technology here.

MS SOOTER: Great. Yeah. So interrupts are definitely not a complicated concept, and I'm sure they do come up.

THE COURT: That's why they let me handle them. That's like I got the patents dealing with this technology.

MS SOOTER: Well, there I guess are fairly a number of aspects of interrupt handling, and in this particular patent we're dealing with a particular aspect of interrupt handling having to do with the prioritization of pending interrupts. And as Your Honor knows, interrupts can come from any sources. They can come from hardware or software and they simply cause the processor to switch what it's doing from one task to another task so that it can handle this pending interrupt. And what we're really going to talk about now is if you look at this diagram, you may receive an interrupt -- and I'm on Slide 6 -- from a keyboard, for example, and then the interrupt interrupts the processor and causes it to execute a program and handle the interrupt. That much you know.

THE COURT: Yeah.

MS. SOOTER: And the part I want to focus on is what happens in between that key press and the time that the processor actually shifts over to the interrupt handler. In other words, what happens in this red arrow here on Slide 6?

And the patent calls that an interrupt circuit. So we'll talk a little bit about the different components that are in the interrupt circuit, and feel free to speed me up if I'm covering --

THE COURT: No. This is very helpful.

MS SOOTER: Okay. So here's what the patent describes generally is happening during this interrupt circuit, and it also states that much of this was already in the prior art. So when you get an incoming interrupt like a keyboard press, then that incoming interrupt is stored in an interrupt register. And in this flow diagram these cylinders depict storage devices or registers. So in this particular example the keyboard press would be stored in the interrupt register. So, for example, if you had four different interrupts that all came in at the same time, they were all pending interrupts, they would first be stored in the interrupt register which would then store a note that all four had occurred. The next thing that happens is -- that the patent describes happening, and this is also a common feature of interrupt handling, is that some interrupts are flow through and proceed and others are masked. They're essentially filtered out. And that occurs with the assistance of something called an enable register. The enable register has flags essentially indicating whether different types of potentially pending interrupts are enabled or disabled, and those flags can then be used by an and gate to determine whether or not an

interrupt that was received should be masked out or filtered or whether it should be passed through to the next step. If it was masked, it stops there. If it was not masked and it's enabled, then it proceeds to the next step and it's stored in a pending interrupt register.

So here, since we had four interrupts coming in and only two of them were enabled in this simplistic example, the keyboard and the mouse, those two pass through and were stored in the pending interrupt register. Then now we have two pending interrupts. So now we have the question, in what sequence should they be processed? And that's where interrupt prioritization comes in. So hypothetically you may have priority levels assigned to these interrupts. And in this case you have a 1 assigned to the keyboard, and that's the highest priority, and a 4 assigned to the mouse. So presumably 1 would be processed first. And those priority levels for the potentially pending interrupts are stored in a priority register, and that's the information that's used to assign priorities to or to prioritize those incoming interrupts.

Now, what the patent describes is that that prioritization scheme or the set of priorities may change depending on the system mode. So you may have a high power or a high performance mode. You may have a low power or, say, battery mode, and depending on the modes, you may have different interrupt priorities.

So in this particular simplistic example on Slide 16 you can see that just hypothetically in a high performance mode you may put your disk drive as the highest priority and the mouse as the lowest, and in a low power mode you may switch up the priorities.

And so the patent describes all of that as the background of the invention. It already existed before the patent came along, and that's where the '025 patent comes in.

The '025 patent is entitled, hardware managed context sensitive interrupt priority level control. So as you'll see as we go through the patent and we walk through it, it uses hardware to manage the interrupt priority levels based on context. It's sensitive to the context or modes that the system is operating in.

So the patent described a problem here on Slide 19 and it said -- it says that interrupt priority levels have conventionally been controlled by software. So historically interrupt prioritization was controlled by software, and that means that any changes in the prioritization of interrupts requires additional time and programming complexity to switch the prioritization by rewriting the interrupt priority registers.

Accordingly, there is a need for improved interrupt controller that allows interrupts to be quickly and efficiently prioritized and a need for a high efficiency interrupt

prioritization scheme that allows interrupt priorities to be dynamically controlled and adjusted. So the patent is saying, historically you've used software to change interrupt prioritization schemes, but we need something that's more quick and efficient that still allows dynamic control of interrupt priorities.

The patent then describes the alleged solution to this problem, and they describe it as a hardware mechanism. A hardware mechanism is provided to adaptively prioritize interrupts based on the current mode or context, and it goes on to say, by providing multiple interrupt priority registers, interrupt priority registers may be switched automatically when there's a change in the mode or operation.

So what does that look like? Now, as you can see on Slide 21, instead of just having one interrupt priority register that's storing the priorities to be assigned to the incoming interrupts, now there -- in this example there are two. So there are two registers presumably each -- that each apply to a particular system mode and that each have a set of interrupt priorities that will be used depending on the mode. And then there's a switching or a multiplexer circuit, as the patent calls it, that selects and passes the contents of the interrupt priority register corresponding to the current mode or context.

So as again, a simplistic example, in a first mode you might have a switching circuit that connects a first priority

register, and this is the one you're in a high performance mode, but in another mode where you're in a battery or low power mode, then the switching circuit might couple the second priority register to the priority encoder so that the different set of priorities are used to assign priorities to the incoming interrupt. And that's essentially what the patent describes here where it says the priority encoder module receives the contents of the priority register that are selected by the multiplexer circuit and then it selects and forwards the interrupt to the CPU after it's prioritized.

This conceptual diagram flowchart on the left that we've been looking at corresponds to the patent's Figure 3, and you can see that we've color coded the different registers. For example, you have the incoming interrupt. It's stored in what the patent calls a source register. The patent also describes in green the enable registers that we talked about. Those are passed through the and gates that are used to mask out the disabled interrupts, and the ones that pass through successfully are stored in pending interrupts -- pending register, and then the interrupt priority registers that store the different prioritization schemes are down here in purple, and the mode selector is used to select one of the interrupt prioritization schemes to then assign priorities to the pending interrupts.

And that's really the overview of the technology which

kind of feeds into what we'll talk about with the claims. So let's go to Slide 30 of the deck.

This first term is found several places in Claims 1 and 9. The priority level information associated with the system mode for each of the one or more interrupt requests. We maintain that this should be construed to mean the priority level information associated with a system mode for each of the one or more potential interrupt requests, and VLSI says plain and ordinary meaning. And it really is -- the fight really is over the word "potential," as you know.

THE COURT: Sure. Let me ask you a couple questions.

MS SOOTER: Sure.

THE COURT: Are capital N and little N the same thing?

MS SOOTER: Let me look for a little N. I know what you mean by capital N. I do not believe so.

THE COURT: And we're looking at Figure 3?

MS SOOTER: Right. Actually, let me think about that. And I know what you mean. I think you're referring to the capital N that's in the specification?

THE COURT: Yes.

MS SOOTER: In the written description where it's saying that there are N different types of priorities basically?

THE COURT: Yes, ma'am.

MS SOOTER: It does actually look as if there -- that is probably the case. I'll -- you know, when I sit down I'll go

back and look at the description of the figures a little more closely, but in looking at this -- let me start here. Perhaps this will help. In rereading the patent, I saw that several times within the patent it talks about having a number of bits. So each bit represents one -- essentially one type of interrupt --

THE COURT: Right.

MS SOOTER: -- that the system could receive. So, for example, in the source registers if you have eight different types of interrupts, you would have eight bits, and one of those bits would get flipped if there was that type of interrupt that was pending. Similarly in the enable register you would have that many bits so that each type of interrupt would have an enable or disable bit associated with it and then you would be able to and those bits together with the 308 and gates that also have N of them and it does look like given that there's 0 to N minus 1 enable registers, it is likely that the little N is the same as what the spec is talking about with a capital N.

THE COURT: Meaning number of interrupts, right?

MS. SOOTER: Exactly.

THE COURT: As opposed to priority definitions?

MS SOOTER: Exactly.

THE COURT: And then if we could go to Column 4.

MS SOOTER: Yes.

THE COURT: And go down to Line -- let's see. Let's start at Line 62.

MS SOOTER: Okay.

THE COURT: However, on chip interrupt requests may also be received from the various peripherals such -- probably as -- there's probably an "as" missing there, but such as -- these guys need to learn how to spell check.

MS SOOTER: Yes.

THE COURT: Which is only the value I could add to drafting patents is maybe if they let me read it I would be able to do it.

But such as the timer module 16 and/or serial module 18 which may feed one or more interrupts 202. The interrupt source register 204 selectively stores all interrupt requests received via the physical conductors or from on chip sources or alternatively routes that received interrupt requests to the CPU, and it goes on. What do you understand the word "selectively" to mean? That's on Line 65.

MS SOOTER: Well, off the top of my head that's a difficult question to answer. I can tell you that this part of the patent, as you probably already know, is just saying that you can either store the interrupts as flags in that interrupt pending register -- in that -- let me make sure I get the name right -- the source register or you can just pass them through essentially instead of I think latches rather than storing them

in a register. I think what I would say is that this is probably harkening back to the part of the patent where it's talking about flipping the bits for the interrupts as they're received. So, again, if you have eight, then -- pending interrupts, then you could flip a bit, but I don't think that the patent is necessarily in this part of the patent where you're talking about storing the interrupts as they're received would be limited to that, and that's not really necessarily -- and I -- I think what where we're going here is what we mean by potential, but what I would say is that you don't -- the patent and the claims in particular aren't necessarily being -- this part of them that's disputed aren't really directed toward that part of the figure, the source registers, and the patent says that that -- there are really -- you don't even need the source registers necessarily unless the claims require them.

THE COURT: Can the number of interrupt sources be greater than capital N?

MS SOOTER: I think the patent is using the capital N to represent -- in the embodiments talking about to represent the number of potential interrupts -- types. Now, that's assuming --

THE COURT: Which is a way -- I'm sorry. Which is a way of saying that capital N is all possible interrupt sources?

MS SOOTER: Yes. That have been configured in the system.

THE COURT: Not just those currently defined or present in

the machine?

MS SOOTER: As in -- by present in the machine, do you mean having occurred?

THE COURT: Yes.

MS SOOTER: I believe it is all possible pending interrupt types. Yes. Now, some machines may have more potential interrupt types than other machines, but it's whatever is possible to occur in that machine.

THE COURT: Give me one second.

Josh probably knows this, but I don't from looking at it. What is NXP? Is that N times something?

MS SOOTER: Oh, yes, Your Honor. So that's funny that you should say that because it's also, I believe, a company, but --

THE COURT: No. That's -- and but it was -- it was used before it was the company. So I was guessing that was not it. So but I -- I don't know what NXP meant.

MS SOOTER: Well, I believe that the patent describes that there can be P bits associated with each priority and each -- the priorities apply to the potentially pending interrupts and then each priority may have a multi bit indication of its priority. So let's say, for example, you had four priority levels.

THE COURT: Yes, ma'am.

MS. SOOTER: That would be two bits because there -- you can represent four different values with your two bits. So you

might have the two bit code encoding your four priority levels and so that would be the P in the NXP. So I think it's N times P.

THE COURT: Got it.

MS SOOTER: Yeah.

THE COURT: Okay. And I interrupted you. You can keep -- if you remember where you were, you can go back there. I apologize.

MS SOOTER: That was -- no. I'm glad you asked. Well, let's actually keep --

THE COURT: And I think what you had just said was -- and I agree with you -- is that the fight is really over, you know, the addition of -- y'all's addition of one word to what the claim term already says.

MS SOOTER: Yes, Your Honor. And, you know, we do believe that the word "potential" in this particular phrase is appropriate based on both the prosecution history as well as the patent's repeated use and description of what we're talking about here and so let's actually talk about -- let's orient ourselves about what we're talking about, what part of the claim we're talking about and -- here on Slide 31. What we're talking about we're defining the term priority level information associated with a first or second system mode for each of the one or more interrupt requests.

And this priority level information that we're defining

right now is if the patent -- this claim says that it's stored in the interrupt priority storage devices. So what we're talking about right now is what's stored in the interrupt priority storage devices. And so what we need to do is look at what the patent says about what's stored in the interrupt priority storage devices, and the same is true on Claim 9.

So looking at Slide 33, we have here just an excerpt from the patent. It's Column 2, Lines 64 through Column 3, Line 22, and it tells us what's stored in the interrupt priority registers. And in particular here the patent tells us that first of all, as we know, one or more interrupt priority storage registers are provided and those are shown in purple on the left and the text is highlighted in purple. Those are provided for storing priority values corresponding to each of the potential pending interrupt requests, and that's the NXP that you were talking about. So there are N of them and each interrupt priority level may have P priority level bits associated with it, thereby enabling prioritization of the enabled pending interrupt requests. So when an interrupt is received and when it is -- before it is provided to the CPU to be handled, it is prioritized and it's prioritized by using the information stored in the interrupt priority registers which is why it's logical that the interrupt priority registers store priorities for the potential pending interrupt requests. In fact, that is exactly what the claims tell us.

If you keep reading Claim 1 here on Slide 31, you can see that you -- that the claim requires providing the logic circuitry with priority level information. That's the priority level information we just talked about corresponding to the mode signal where the logic circuitry -- this is the important part -- uses the provided priority level information to prioritize one or more of the pending interrupt signals. So that's the -- now, this interrupt priority level information is the information that's stored on the interrupt priority storage devices so that it then can be used, according to the plain language of the claim, to prioritize the pending interrupt requests when they arrive.

And because the patent does explain over and over again that the priority levels for the possible pending interrupts is what's stored in the interrupt priority registers, then interpreting Claims 1 and 9 that way is entirely consistent with the patent. Now, we recognize that we are adding the word "potential," and we do -- we anticipated the arguments that VLSI would make in response. Of course we knew that they would say that we were adding a word to the claims, but we're cognizant of the law surrounding claim interpretation of course. We understand that in order to add a word to claim, then it needs to be the proper interpretation in view of the intrinsic evidence, including the prosecution history. And the prosecution history here actually dictates this result.

If you look -- let's start with Claim 9 because they're accusing us actually of inserting several words into Claim 9. So it's not just one word. Potentially it's many words. So let's start with that one. This is a prosecution history for Claim 9 here on Slide 36. You'll see the -- on the left the actual language of Claim 9 is just priority level information associated with a first system mode and priority level information associated with a second system mode. And as you know, we are interpreting that to require that that be for each potential pending interrupt, and that is not our language, Your Honor. That's the language of the original patent owner when the original patent owner sought to obtain these claims from the Patent Office. There -- and so on the right is an excerpt of the original patent owner's representations to the Patent Office. There they say Claims 9 through 14 and 16. So the very claim we're talking about are not obvious over Kershaw and Chou. And they're telling the Patent Office in response to the examiner's rejection of those claims as being obvious over this prior art, applicants respectfully request reconsideration and withdrawal of the rejection because the cited art fails to disclose or select -- suggest applicants disclosed interrupt handling methodology.

So when -- in their briefing VLSI says that we're misinterpreting this because all the patent applicant was doing was describing the invention, but that's not actually what's

going on. What's actually going on here is that the patent applicant was telling the Patent Office how to construe the claims because they wanted those claims construed in a way that the Patent Office would grant them.

Well, how did they describe those claims? Again, Claim 9, the patent -- the original patent owner said, as described in the application, the interrupt priority registers are provided for storing priority values corresponding to each of the potential pending interrupt requests depending on the system context.

So, like I said, this is the patent applicants' words, it's their description of this claim and what this claim requires to the Patent Office.

This was similar to what the patent owner said about Claim 1, which we're also construing here. Claim 1 is only one word that we're fighting about, and that's the word "potential." And here you can see that they were making the same argument with regard to Claims 1, 3 through 8 and 17 through 20. They're, once again, telling the examiner, you should not reject these claims. Let me tell you what they really mean.

And what they say is -- looking down to the -- they're describing both. They say -- looking down to that second excerpt, as described in the application, the interrupt priority registers are provided for storing priority values corresponding to each of the potential pending interrupt

requests depending upon the system context, and then they say it again, potential pending interrupts and possible potential pending interrupt requests.

Now, what happens? The very next thing that happened in prosecution is that the patent examiner came back and said, okay. I hear you. The Patent Office said reasons for allowance. They granted the patent right after that. They said the examiner interpreted the claims in light of the specification and in further view of applicants' persuasive argument.

So, again, it's not a description of the patent or the specification generally. It's the applicants' persuasive arguments as to how to interpret the claims and the patent examiner said that it was persuasive. And what was persuasive? Exactly what we've been talking about. The patent examiner said, as described in the application, the interrupt priority registers are provided for storing interrupt or priority values corresponding to each of the potential pending interrupt requests.

So we'd represent to Your Honor that all we're doing with this language is asking the Court to construe the term -- these terms in these claims exactly how the original patent owner construed these terms and these claims in order to obtain this patent. And I would just add, Your Honor, that --

THE COURT: Could you go back to that?

MS SOOTER: Sure.
THE COURT: Give me one second on your slide.
MS SOOTER: This is Exhibit 17 at Page 2, and we're on Slide 38 for the record.
THE COURT: Thank you very much.
Okay.
MS SOOTER: Now, the one argument I would go ahead and address now that VLSI makes is that the word "potential" does appear in Claim 17 but it does not appear in Claims 1 and 9, but the case law says that claim differentiation -- first of all, this isn't actually a claim differentiation argument because we're not talking about independent and dependent claims. They just point out -- their argument is if we wanted to say potential, we knew how to do it. Our counter to that is --
THE COURT: Well, not only that. That's -- and you -- and that's why if you'll go to the page before. That's what I was actually looking at is I get that -- I get that the examiner writes, the reason for allowance -- he includes the word "potential" pending interrupt. I get that, but -- but he was aware that -- but the way I understand this works is if the examiner had wanted to require them to include the word "potential," he could have made them do it. I mean, it's -- I mean, to me this actually hurts your argument that he wanted that -- I -- he or she. I'm not sure, but I'll say it was a

he. That the examiner was -- I mean, I think examiners are sophisticated enough that if the examiner believed that the word "potential" was the reason for allowing that, he would not have allowed them -- it to be omitted in the claim -- he would have done -- the claim would read the way you want it to read if the examiner had required that word to be in there for it to be allowed. Even though I get he has it in reading it. Now, we'll never know why he allowed it or why he wrote this. I'm just saying -- I'm telling you the way my logic works is you want to -- you want me to essentially rewrite the claim term to add a word that the examiner was aware and did not require them to put in it.

MS SOOTER: Thank you. That was -- I appreciate you explaining that and that was helpful. So my response to that, however, is that there is an entire doctrine of case law under Phillips that -- as you know, that says --

THE COURT: I only know about four cases, and Phillips is one of them. And so...

MS SOOTER: One thing that Phillips absolutely says is that you really do need to read both the specification and the prosecution history and try to discern what the invention was, and so there are many, many, many cases in the Federal Circuit as well as the district courts that are doing just that. They're not looking -- they're not stopping and looking at the claim language and then ending the analysis. And so these

cases that you have that are interpreting the claims in view of all of that intrinsic evidence are repeatedly doing exactly what we're doing here. The entire body of case law that -- you know, if the examiner required the patent owner to rewrite a claim every time the patent owner interpreted the claim in a way that they relied on or it disavowed some scope or disclaimed some scope or changed the interpretation, then we wouldn't even have that body of case law.

THE COURT: But the reasons for allowance -- check me on this. That's part of the intrinsic evidence, right?

MS SOOTER: Yes.

THE COURT: And, again, the examiner who allowed this claim to be issued without the word "potential" in it was -- I'm just having a hard time believing that the examiner didn't do his job and require the applicants to put into the claim every word that needed to be there, and I feel like you're asking me to replay the role of the examiner here which I'm reluctant to be.

MS SOOTER: I understand.

THE COURT: He had -- the examiner had the chance to require this, and the reasons for allowance make it patently clear that he was aware of the issue you're raising and yet he didn't do it.

MS SOOTER: I hear what you're saying and I won't belabor the point. I'll just state for -- our position is that this is

one of a very common type of example where the patent owner interpreted the claim to the Patent Office and the Patent Office relied on that, and it's not even one where you have to read between the lines to think about what the patent owner might have or might not have relied on in the patent applicant's arguments. He actually tells us what he relied on and he said that he found those persuasive arguments and as a result -- and he actually explains what they are and one of them is that the patent owner interpreted its own claims to require them to store each potential interrupt request. So that is our reading of this. That's our understanding of the case law as well.

I will say, Your Honor, that there are just a whole slew of cases that are talking about examining the intrinsic evidence in view of -- in order to obtain an interpretation of the invention. And there was just a case today actually that came out of the Federal Circuit called Techtronic Industries vs. ITC that reiterates much of what we said in our brief which is that you really do in many cases obtain the meaning of the claims from the intrinsic evidence from types of statements exactly like this.

THE COURT: But aren't there a lot of Federal Circuit cases that tell you to look at the claims first and then go to the spec?

MS SOOTER: Regardless of what you look at first, you have

to look at all of it to discern the meaning from the claims, the written description and the prosecution history. And the one today made clear several quotes. And that's Case No. 182191 for the record out of the Federal Circuit.

Disavowal must be clear, but it need not be explicit. And this, we would argue, is clear. Disavowal may be inferred. The purpose of claim construction is to capture the scope of the actual invention. So I know that VLSI quoted several times in its briefs the kind of adage that claims claim, but that really should not be taken to -- as Your Honor is obviously well aware, to be the end of the analysis. And we would submit that this was pretty persuasive evidence of what they really meant. And with that, I'll stop.

THE COURT: Thank you very much.

I'm going to find -- I'm not going to add the word "potential" to either of the claim terms.

So we have our final -- and it's not just so I get to hear from Mr. Ravel more quickly, although that played a -- that did play a tiny part in it. This is the final claim term, is it not?

MS SOOTER: No, Your Honor. There's also interrupt priority storage device.

THE COURT: I'm sorry. Help me out. Do I have two more?

Yes. I'm sorry. You're right. I had -- I tell them not to print on both sides of the page because I can't find

anything. So the next one up is storage device for storing priority level; is that correct?

MS SOOTER: Yes, Your Honor. And, you know, we make similar arguments on this. Let me just say, you know, for 30 seconds here. We make similar arguments here, but we think in this case the disavowal at the Patent Office was explicit. It was express, and the patent owner said many times in the patent and before the Patent Office that the priorities should not be rewritten by software, and that is the point of the invention, but I don't want to belabor the point, and if Your Honor would rather not hear more about that, I'm happy to turn it over to the star of the show.

THE COURT: No. No. I was -- I know we have the show pony coming up last.

(Laughter.)

THE COURT: But I'd certainly -- if you have something -- I've got all the time in the world, and if you have certainly any arguments you want to make, I'm much more open on this one than I was on the -- the previous two I had -- I always have a hard time when people are trying to persuade me to take language and do what you were doing. But no. You're welcome to make these arguments.

MS SOOTER: Okay. I think, Your Honor, in view of, you know, the case law that I was just describing and the purpose of the invention that I mentioned earlier which is -- was

really to identify a way of changing interrupt prioritization schemes when the -- when the system mode changed in a fast, easy, low latency manner, the patent described the invention as providing multiple prioritization schemes stored in hardware rather than rewriting the prioritization scheme whenever -- by software whenever the mode changed. And I would just point out, Your Honor -- let's go to Slide 18.

THE COURT: Okay.

MS SOOTER: This one I think is an even stronger prosecution history, and it is, we believe, an express disavowal of claim scope in order to obtain these claims. The patent owner said here -- they emphasized once again that in Claims 1, 3 through 8 and 7 through 20, they discuss the interrupt priority registers. Then they said that the -- they enabled -- this is Slide 18. They enabled the prioritization of the enabled pending interrupt request while eliminating the requirement for software management of priority level changes during context switches.

And they specifically describe the prior art that the claims had been rejected over by saying that Kershaw's priority value managers are clearly and repeatedly described by Kershaw. Kershaw's a prior art patent. As being software based priority control mechanisms.

But they went on to say, there is a very real difference between the claimed invention and the Kershaw disclosure in

that the Kershaw uses the operating system software to set the interrupt priority values, whereas Claim 1 specifies that different interrupt priority level information for each requested interrupt request is stored in interrupt priority storage devices. So, in other words, Kershaw's use of the operating system software as shown on Slide 19 was a very --

THE COURT: Could you go back?

MS SOOTER: Yeah. Sorry.

THE COURT: So first just for my court reporter, Kershaw is K-e-r-s-h-a-w.

So I'm reading what you're reading and -- on Slide 19, does the -- and this is the problem with the English language. The way it's phrased, I can't tell if this means that -- and I want to hear your argument on this and of course from VLSI. Does this mean it cannot use the software at all?

MS SOOTER: Thank you, Your Honor. So this -- going back to the claim language itself, let's go to Slide 4.

THE COURT: Okay.

MS SOOTER: What we're construing right now are the storage devices for storing priority level information. The claim requires a first interrupt priority storage device for storing priority level information associated with a first system mode and a second interrupt priority storage device for storing priority level information associated with a second system mode. So what we're saying is that when the mode

changes and you change from one priority storage device to the other, you're not doing it by rewriting the priorities with software. That's what we mean when we say the priorities are not rewritten by software when the mode or context changes.

THE COURT: So let's say the interrupt priorities changed during or within the execution of a specific mode. Under your construction, would software be allowed to be used in any way to rewrite the priority levels?

MS SOOTER: Yes. I think so, Your Honor. So, for example, if I understand your hypothetical correctly, if you're just always for, I don't know, three minutes operating in the same system mode but something comes along and for some reason your operating system needs to change the priorities because from -- you know, you got an update to your software -- your operating system or something. I don't know. And so from here on out you're always -- your interrupt priority levels are not going to be what they used to be because there's some different policies. Let's say for example there's a new interrupt type and so you need to add that interrupt type to the priority information. Then you would need an interrupt priority level for that new interrupt type. You could add that with software, but what we're saying is that when you switch system modes, the whole point of the invention is to use a prioritization scheme by switching the hardware from one set of -- one storage device for storing priority level information to the other.

THE COURT: Okay.

MS SOOTER: And that, we believe, is supported by that clear and unambiguous disavowal of rewriting the priorities by software in order to change the mode as opposed to switching with the software.

THE COURT: Okay. Thank you, ma'am.

MS SOOTER: Thank you.

THE COURT: Yes, sir.

MR. HATTENBACH: Good afternoon, Your Honor. Ben Hattenbach for VLSI. It's good to see you again.

THE COURT: You're just as much of a show pony as Mr. Ravel. I looked forward and hoped all day you would get up.

(Laughter.)

MR. HATTENBACH: All right. So let's see. I have a hard time even figuring out where to begin. We appreciate the questions from the Court yesterday, but --

THE COURT: However, let me just say -- yeah. I was going to say you are beloved and respected in the courtroom by everyone except for my court reporter who may respect you but doesn't love you. So if you would go just a little slower, you'll make her and all of us happy.

MR. HATTENBACH: Absolutely. I'll try to be a slower show pony.

THE COURT: Okay.

MR. HATTENBACH: As I understood the questions from the Court that Dr. Yi conveyed to us, I think they were all about the term "potential," and we wanted to address them, but we won't, given the Court's order. If there were any remaining questions on that front, I would be happy to try to address them, but I don't think they pertain to the hardware addition.

THE COURT: They don't, I don't think.

MR. HATTENBACH: And I also was going to go through a bit of a tutorial, but given Your Honor's statements at the beginning, I will save us the time there. I will just note that a tutorial that we were given and the description of the positions that we were given was all limited to essentially one part of one preferred embodiment. The rest of it was just cut out of the patent as though it didn't exist, and of course there are many cases that say, for good reason, you can't interpret patents that way by ignoring the parts of them that don't really work for your attempt to rewrite the claims.

Let me cut to the chase here. On Slide 12 of Intel's presentation they really set forth, I think, the crux of their argument, and it says, upon changing mode, software does not, underlined, does not rewrite the priority levels. That's the key of their argument. They're trying to say put a hardware limitation in because software does not rewrite the priority levels.

I'd just like to refer Your Honor to the patent at

Column 6, Lines 60 to 63 where it states, priority values may be updated or changed under software control. That's the opposite of what they're telling you about how this -- how this technology works, and they left it out of their presentation, and, again, you can't limit claims based on one preferred embodiment when it's absolutely inconsistent with another.

If we could go to Slide 259.

Let me start there on VLSI's slides. The first thing I will note is much like their effort to put in a -- the potential limitation into the last claim element, they're trying to put in a hardware limitation into this claim element. You can see on Slide 260 a comparison of the actual claim terms on the left and their proposal on the right which essentially repeat all of the technical terms in the term -- in the term being construed. There's nothing unclear about them. They're just adding to them. And the language they're adding is the language in red, and of course, and I won't belabor this point because I'm sure Your Honor is familiar with it. You don't interpret claims by just adding to them. There has to be some textual basis in the claim that you're using as sort of a springboard. There has to be a word on the left of this chart that you're saying means something that you're trying to add on the right. And here there can't be because if you cross off all the words on the left that also appear on the right, all you'll be left with is Intel's addition. It sort of identifies

04:46 itself for us.

And I'm going to skip over the authority going back to 1895 which we heard about earlier today talking about slippery slopes and the like.

There's no doubt that if the inventors had wanted to limit their claims to hardware only embodiments, they could have done so. If we look at Slide 264, we'll see an example of a couple of claims where the inventors specifically call out types of hardware, logic circuitry, multiplexer circuits, selection circuits, and there are other examples. So if they wanted to limit it to hardware, they certainly knew how to do so and they chose not to.

Intel's rewriting the claim would also exclude preferred embodiments. If you see on Slide 266, this is actually the language which I was referring to earlier where it specifically says -- I mean, it couldn't be any more clear. The assigned priority values may be updated or changed under software control. Now, it does continue. It says, however, there is a latency issue when using software. Well, as with any other engineering problem -- engineering is often, as you probably know, about optimization. Some things work better in some respects and worse in others. Well, software's very flexible. It allows you to change very easily how the system operates just by putting in a new program or making a slight edit to the program, whereas with hardware if you want to change how it's

operating, you need to fabricate an entirely new piece of hardware which could take months, if not years in the case of the sort of hardware that Intel makes. So the point here is the patent talks about benefits of flexibility. It talks about benefits of speed. Flexibility's provided by software. Speed is provided by hardware. And it says you can do either one. Here it's saying you can do it under software control. There are other parts that talk about it being done with hardware. And ultimately that's just a design choice for purposes of optimization for particular applications, but that isn't present in the claims and it doesn't limit the claims and it shouldn't be added to the claims.

There are other examples which -- let me just skip it over because I think we've hit the main point, but there are other examples where software is involved in changing modes which then result in changing priority values which Your Honor asked about earlier. Those are on Slides 268 and 269.

And then let me just move on here. So here are some of the pros and cons discussed on 271 that I was referring to earlier about flexibility that software provides and speed that hardware provides. It never says you have to do one or the other.

And here on Slide 272 there's some case law that just -- it's just sort of common sense. It says a patentee's discussion of shortcomings is not a disavowal. Often

shortcomings, as I said, are accompanied with benefits in other respects.

They would also -- as they're construing the claim, as they're limiting the claim, it would exclude all of the preferred embodiments they didn't discuss, but there's more. There are two terms actually at issue here. One talks of storage devices and the other talks about priority levels. You can see on Slide 276 those claims, Claims 1 and 9, speak of storage devices. Claim 17 is directed to priority levels and yet they're giving essentially the same interpretations. It's a few wording differences but not wording differences that would be explained by the differences in the words they're actually purporting to interpret. So that's yet another problem. And of course the use of two terms in a claim requires that they connote different meanings. It's just common sense.

THE COURT: Where would you say that the hardware and software interface is disclosed in the patent?

MR. HATTENBACH: Hardware and software interface. Well, that's a tough one. I mean, I think -- I think everywhere they talk about software. Probably a person of skill in the art would understand that that software is going to be interacting or controlling some aspect of the hardware operation where it's a mixed hardware and software system. I think some examples that come to mind -- let me -- give me one moment here. I have

something in mind, but I need to find the cite for it.

Okay. Could we go to 26 -- let's go to 268. So I'm not sure if this is the level of detail that you're looking for, but, for example, it talks about context switching based on an operating system.

THE COURT: Slow down just a little bit.

MR. HATTENBACH: Sure. The patent speaks of context switching based on the operating system. It talks about context control bits in Column 7 at Line 61 to 67. And, generally speaking, the patent describes, and people of skill in the art would understand that software can write to various registers and storage devices and change modes and the software can receive interrupts.

I think there's more on -- if we go back to 268. There's also some description here in Column 5 and Column 6 of how certain things are not only preprogrammed but then can be updated under software control. That was also something that we discussed in the briefing. There was an argument that the system didn't allow updating. It just allowed programming in the first instance, and we point out -- and it's here on the second portion of the patent on Slide 267 where it shows, no. Indeed, there can also be updating under software control. I'd say it's a combination of all those areas together with what a person of ordinary skill in the art would understand about a system like this.

THE COURT: Very good. Did you have any other points to make?

MR. HATTENBACH: Sure. Just one more point which is on the prosecution history. The sections that counsel was relying on a moment ago actually weren't, for the most part, discussing the claim language. They all used -- they all were discussing what was described in the application as opposed to what was claimed in a particular claim, and so I don't want to bring up Slide 18 and take up the time, but it -- the quote begins with, as described in the application. And it continues on. It says in selected embodiments. Well, talking about how selected embodiments operate is very different from saying, let's talk about a particular claim and particular claim language and here's what it meant. That never happened. There are references to -- let's see. There was a reference to a software based priority control mechanism. My understanding of that is it was a 100 percent software controlled system that operated 100 percent using software, and that's not what the claim is directed to. And so it was entirely appropriate to differentiate that. The claims we're speaking of today require storage devices as part of this process, and both parties agreed -- it's in the briefing and we affirm it now -- we all agree a storage device is a piece of hardware. And so what's actually claimed, if you look at the claim as a whole, is really quite different from what was differentiated properly

during prosecution.

If there are any other questions or concern about the prosecution history, I'd be happy to try to address it, but otherwise I will yield the time back to the Court.

THE COURT: Counsel?

MS SOOTER: Let's start with Figure 3, please. So I believe that the answer to the question of the hardware software interface is this mode context selector, 26. So basically the operating system can change the mode or the context and thereby changes the input to this switching circuit here which then is hardware and then it selects a different register which are hardware, and that's all in hardware. So the interface to the operating system would be the mode or context selector in this figure. So that was my take on that question if I understood it properly.

Now, let's go to Column 6 at Line 60 the last paragraph. Last partial paragraph.

This is the part that counsel relies on to say that software -- that the priority values may be updated or changed under software control, but it says right in the middle there starting at the end of the line in about the middle, by implementing the interrupt priority register 212 as a read write register, the assigned priority values may be updated or changed under software control.

Now, first of all, it does go on to disparage that

technique, but let's look at -- counsel did start his argument by saying that there were two embodiments here, and this 212 is the first embodiment. It's Figure 2.

If we could go to Figure 2.

Figure 2 has 212, has interrupt priority register. It has one of them, but that's not the claimed embodiment in Claims 1 and 9.

If we could go to Claim 1.

Claim 1 requires two hardware interrupt priority storage devices. That's not embodiment shown in Figure 2 that -- the text that VLSI relies on repeatedly refers to. The text that VLSI refers to is simply not the embodiment claimed in Claims 1 and 9, and there's an entire body of case law, as Your Honor is well aware, regarding unclaimed embodiments under the Johnson and Johnston line of cases, and this is one of those cases where even if -- and, frankly, Embodiment No. 1 is very explicit in saying it can have one or more, but even if that was an embodiment, that's not what Claims 1 and 9 are claiming because they require two. And the patent goes on at the end of Column 6 to disparage the software use of writing the interrupt priorities and say, we prefer the hardware, and then it spends columns and columns and columns talking about the hardware, and then finally it all culminated in prosecution.

If we could go to our Slide 22.

All of these statements, all of this disparagement in the

patent itself of the prior art, software, interrupt control, techniques and the teaching and the solving of the problem using hardware all culminated when the Patent Office granted these claims and the patent examiner said in response once again to the prior patent owner's representations that -- about the scope of the claims, the Patent Office said, the examiner interpreted the claims in light of the specification and in further view of applicants' persuasive argument that Kershaw uses the operating system software to set the interrupt priority values, whereas Claim 1 specifies that a different interrupt priority level information for each requested interrupt priority request is stored in devices. That's the hardware.

And then he goes on and at the end he emphasizes that part of the argument that he relied on and found persuasive was that the claimed invention eliminated the requirement for software management of priority level changes during context switches. And all we're asking, Your Honor, is that the current owner of this patent be held to the word and the representations of the original owner to the Patent Office in order to obtain this patent.

MR. HATTENBACH: I'll be quick, Your Honor, but I will speak slowly.

Can we go to Slide 220?

THE COURT: Actually, I'm going to go with plain and

ordinary meaning.

MR. HATTENBACH: Thank you, Your Honor.

THE COURT: You're welcome. I did that to save my court reporter.

(Laughter.)

THE COURT: However, let me make clear on the record Intel's arguments are not lost on the Court. And we will -- when we get out our order that tells you the basis for our constructions, I feel that Intel will feel -- will understand that what they've argued has been heard. We will -- as part of the plain and ordinary meaning construction in this case, we will reflect what occurred during the prosecution history of the case.

Mr. Ravel? Please tell me I get more binders.

(Laughter.)

MR. RAVEL: We -- you have all of them already.

THE COURT: Okay.

MR. RAVEL: I'm Steve Ravel for Intel, and, first of all, I'd like to thank the Court for putting me and my 1977 political science degree at ease, and more to the point, I'd really like to thank the Court for its assistance in managing expectations for my appearance here in front of you today.

And I want to start on the slide that's before you No. 43, and most specifically with the underlined red the, singular, plurality of interrupt priority storage devices. And we're

going to read this claim from the bottom up, and I think it's very important to read it from the bottom up here because the thing that drives indefiniteness here, the thing that makes this analogy to a real estate legal description not reasonably certain enough to enforce starts there with the singular plurality, and unless I missed it, you will not see this third claim limitation in VLSI's presentation at all. And it is the thing that renders it indefinite and not reasonably certain. It is the thing that puts it over the edge.

So picking up right there with the Court's official video on the anatomy of a patent case and the analogy to a real estate deed, I want to go back dejavu all over again to the 1990s when you were a general civil common-law judge and I was a general civil common-law trial lawyer and our Socratic dialogues included or were actually dominated by discussions about whether language was sufficiently certain in a deed and a contract and a statute to put people on notice and to be reasonably enforceable against them, and I think the tools we developed there will stand us in good stead in determining indefiniteness here today. And a little later on I might expand that real estate analogy to Michael Dell's suburban homestead where he runs regular kind of horses and Arabian horses and maybe use horses as the analogy as an ohmage to Judge Nowlin, but it may not be necessary.

Let's dig into the language. Singular, the plurality of

interrupt priority storage devices. What is the clear road map, the clear antecedent basis for that? Notice that we see plurality of interrupt priority storage devices twice earlier in the claim connected by the conjunctive and. So how do you square the singular plurality down in the third limitation with the conjunctive and tying the similar limitations in the first two paragraphs? And the answer is you don't.

So to understand in a little bit more formal way why the claim is indefinite, it is helpful to start at the last limitation because there must be an antecedent basis for that last limitation. You have to look up and you see not one but two.

And, Judge, I think we need to slap on those virtual reality goggles that would render you and me something that we would never be in real life, and that is a person of ordinary skill in the art. And so what would a person of ordinary skill in the art see? That there are two places and not one where the term plurality of interrupt priority storage devices is used. And the second use is distinguishable but not in a material way. And I think if you look carefully at the first two limitations, the additional verbiage in the second one does nothing more than make the second of the three limitations a more narrow version of the first. Hence, the analogy to Michael Dell's home place, our person of ordinary skill in the art trying to figure out how big the home place was and what it

05:06 covered and what it included and where the fancy Arabians were
05:06 barned and stabled in the first limitation and any old horse in
05:06 the second limitation. A person of ordinary skill in the art
05:06 would just be hopelessly confused about where to go for the
05:07 Arabian only horses or the any old kind of horses.
05:07 And I probably should have highlighted this sooner. The
05:07 blue underlines are the distinction between the first
05:07 limitation and the second, and they just don't move the needle
05:07 for making the practitioner know where to go. It could be
05:07 read, conceivably could be read as a subset of the broader
05:07 first limitation, but it doesn't provide any clarity.
05:07 VLSI is asking you to do something that the cases don't
05:07 let you do, and that is render either the first limitation or
05:08 the second limitation redundant. Notice as we walk through it
05:08 specifically with the singular the on the bottom they are
05:08 asking you to omit, to strike out either the first limitation
05:08 or the second limitation. So the reasonable practitioner
05:08 doesn't know whether it is one plurality, two pluralities or
05:08 four pluralities. It is particularly based -- on the third
05:08 limitation with the plurality referring to two conjunctively
05:09 linked similar limitations, it's just Intel's position that you
05:09 can't get there from here on certainty, Judge, and let me try
05:09 to diffuse a couple of the things that they are trying to --
05:09 that they're likely to say to you based on their slides. First
05:09 of all, I don't -- I don't like to issue challenges, but the.

How do you get over the problem caused by the, singular, plurality, two conjunctions and two similar limitations? They're likely to cite to you an Eastern District case that says redundancy is just okay and they sure over blow that case. It is a -- it is a -- it's in a footnote. It's in unlucky Footnote No. 13, and it says that you can harmonize a stray whereas or wherefore, but it certainly doesn't stand for the proposition that one can harmonize -- and, again, I hate to stress it too much, but it's -- the bulk of the argument is the two conjunctive limitations coupled with the singular plurality relating back is just absolutely fail to definiteness here.

I also want to mention from their briefing I think today for the first time -- in fact, I know today for the first time instead of saying definite where their expert did opine as to what it could mean, and it -- and they did chide us throughout their briefing for not biting down on what it could mean or rejecting a reasonable expectation, but -- a reasonable construction, but all of that is just self defeating, Judge. When the party that's advocating for certainty use words like "could" or "a reasonable," they're just admitting themselves out of court. I have some other things to say about their presentation, but I'll hold it back for rebuttal, but you just can't get there from here. Two conjunctions and a singular. Can't get there from here.

THE COURT: Mr. Ravel tells me you can't get there from

here.

(Laughter.)

MR. HATTENBACH: I believe I can get there from here. Let me take a shot at that.

Can we put up Slide 294?

This is Mr. Hattenbach again for VLSI. And here's the language that Mr. Ravel was looking at which requires a plurality of certain things and a plurality of certain things which sound an awful lot like the first set of certain things but then also require the language that's underlined in it's either blue or purple there. I can't quite tell. But for each of the one or more interrupt requests which appears twice. So the second providing element is narrower than the first.

And that actually was the argument that I understood them to be making in their brief that these are just duplicative and you have to provide one or two. We can't tell, so therefore it's indefinite. And we responded to that by pointing out that in fact there's some duplication of text. It's certainly not the most concise claim I've ever seen. I'll stipulate to that. But it's not indefinite for that reason that was discussed in the briefing because the second element adds limitations and is therefore narrower than the first.

As to the argument about getting there from here that was raised, let me try an analogy on you, Your Honor. Let's say you have a bunch of apples in your shopping cart and you go

back. You decide it's just not enough apples. You're going to get another bunch of apples. And maybe the second bunch is of a particular type whereas the first bunch is just general -- apples in general. So now you have two bunches of apples, or as a patent lawyer would say, two pluralities of apples.

THE COURT: They would say two pluralities of fruit.

(Laughter.)

MR. HATTENBACH: Very well.

THE COURT: They wouldn't want to be bound to it being apples.

MR. HATTENBACH: If I started speaking like that, I might get thrown out of many stores, but, nonetheless, they would say two pluralities of fruit. And if someone -- you were checking out and the checker said, give me one of those pieces of fruit, you wouldn't say, I don't know what you're talking about. You'd be able to pick one of the pieces of fruit, whether they were apples or bananas or anything else. I think the same applies here. There's a first plurality, a second plurality, and then the element that comes next that he was taking issue with just requires you to pick one of those things. He didn't mention this, but a plurality -- plurality's a strange word in that multiple pluralities are themselves a plurality. And the claimed plurality which is on the next -- it's the next element to follow and it's not on our slide because I don't think they made this argument before, but the claimed -- that element

says, just pick one of the things that were introduced above. It's the two bunches of apples. You just have to pick an apple. I don't think there's anything so unclear about that that the claim should be rendered indefinite. It definitely should be criticized for using excess verbiage. Like I said, we'll stipulate to that. But figuring out what it means to pick an apple from two bunches of apples is not something that's beyond the capability of an elementary school student, let alone a person of ordinary skill in the art even in the abstract. And here it's not being done in the abstract. It's being done in the context of a patent specification that is in accord with what I just described.

And so on -- I don't want to take any more of your time, but on Slide 297 the patent does describe two devices for priority storage, storage of priority information and a -- and a plurality of those devices. Two is a plurality. And that's entirely consistent with our construction of the term. They said in their briefing, by the way -- well, let me address one other issue. In terms of the alleged lack of clarity here. As we've heard many times, and this is the Phillips case that says itself but many others as well have said you have to look at a the context of the particular claim or the particular element. You can't just pluck it out of thin air and look at it out of context. Well, the context here -- and this is what a person of skill in the art would be looking at when trying to

determine, do I need one plurality or two pluralities or something else? They would see, and this is, ironically, enough in exactly the same element that Intel is focusing upon, but they didn't mention this, that when it came to interrupt priority storage devices where the patentee wanted to say I want two of them as opposed to one plurality, they said a first interrupt storage device and a second interrupt priority storage device. And so someone -- if someone was left wondering what was happening here, they would see where multiple instances of a particular type of element were desired was called out in the claim. Where they weren't, it wasn't. And then I think this is in the briefing so I'll just say that at least some redundancy is permissible.

There was also an argument in the briefing that we're asking the Court to disregard the second providing limitation is duplicative. We're absolutely not. Both elements need to be satisfied for there to be infringement. It's simply the case. But when the claims are applied -- and this is more in the infringement side of things than the claim construction side of things. The same language in the claim can be infringed by the same element even if that language appears multiple times. And we had a bunch of cases -- we had a bunch of cases supporting that proposition in our briefing.

To the extent there's any lack of clarity -- and we don't think there is. They seem to think there is. There's an easy

solution here. The law disfavors invalidation of patents. It disfavors findings of indefiniteness where there's another reasonable option, and the most reasonable option here, and we have no problem with it whatsoever, for resolving this dispute is to simply construe the claim. You could say it requires at least one plurality of interrupt storage devices itself comprised of at least two such devices. And that proposed language is on Slide 307, and we'd ask Your Honor if you think there's any lack of clarity, let's just -- let's just get rid of it by adopting a construction that's set forth here, that's completely consistent with not only the claim language but, as I said, the preferred embodiment.

Any questions?

THE COURT: Had you proposed that to us before? I don't remember seeing that.

MR. HATTENBACH: I think we proposed the concept of clarifying any alleged confusion with a construction in our briefing. I don't recall offhand, but I can check to see whether we put that exact language, but that is what we said all along we thought it meant. So I think if you put all of it together, the answer is yes.

THE COURT: And I know I have in my notes as I was going through it and Josh was going through it something that -- along the lines of what about saying something about two devices, but I don't remember if you all submitted something.

MR. HATTENBACH: If you give me just a moment, I can probably track that down.

Well, I don't want to take up your time. It is our proposal it -- I think if it's not set forth explicitly in our brief, it would be inferred from the fact that we said we think this is the right construction all along and that the better approach to invalidation would be to interpret it in the way that we understand it. But I don't recall whether -- I'm just trying to answer your question as precisely as possible whether we actually said, here's how you should interpret it, but we are saying that now.

THE COURT: That's all I need to know.

MR. HATTENBACH: Thank you, Your Honor.

THE COURT: Let me hear from Mr. Ravel.

MR. RAVEL: Judge, I will represent to the Court that the extent of their curative attempts up to this point have been limited to the word "definite." There was not a plain and ordinary meaning. There was not -- there was the chiding of us of being rejecting of what it could be or what the most reasonable reading was, but in terms of a proposed fix to the problem, we saw this for the first time today, not complaining, but this doesn't do the trick on many levels. First of all, it's inaccurate because at least one should really be two. The itself should be each. And I could go on and on about why it's wrong, but the real reason that it's wrong is the case law that

says they're leading you into error when they ask you to rewrite a claim to save it from indefiniteness. I mean, the cases are just legion on that.

Mr. Lee, may we go to Slide 48, please?

I'll match their spec reference that they think is clarifying with a spec reference that we think is equally confusing. So it points in both directions. So I think that's a wash. But what I want to conclude with is something remarkably simple, certainly simple to someone simple minded in the way that I am. And let's go back to the phrase "the plurality." I think we can agree that the "the" must have an antecedent basis, and the unanswerable question and the question that destroys definiteness is, is it the first limitation or the second limitation that is the appropriate antecedent basis for the the plurality? And that's just unanswerable under the four corners of this claim, Judge.

THE COURT: What if they had said one of the pluralities, i-e-s?

MR. RAVEL: I'm quick to point out they didn't, but --

THE COURT: Well, and I -- whether they did or not, they didn't, but I am somewhat taken by the argument that plurality is one of those words where a plurality of -- more than one plurality can be a plurality. You can have -- if you have three pluralities of bananas and you put them on a table, you have a plurality.

05:23 MR. RAVEL: But that argument is -- runs afoul of the, then why did they say it twice? If one plurality could -- why did they have to say it twice? To get to that solution to the problem, they're reading either the first limitation or the second one out. Even if that's right, it doesn't solve that problem.

05:24 That's all I've got absent questions, Judge.

05:24 (Conference between the Court and Mr. Yi.)

05:24 THE COURT: Could we have that -- Mr. Ravel, could I have you back for a second? I'm sorry. I was -- could I have your last slide up?

05:25 MR. RAVEL: This one?

05:25 THE COURT: So we in the first paragraph, providing a plurality, and then in the second paragraph, providing a plurality, and then in the third paragraph it says, one of a plurality, and really if there's an error here, they could have said one of the pluralities. They could say one of either, but it is not -- it is doesn't strain me -- it doesn't cause me too much stress to think that the person who wrote this when he said one of the plurality was talking about either the first paragraph or the second paragraph and -- because it's consistent with what is said after that. One of the plurality of interrupt priority storage devices is what starts each of those, and so that paragraph makes sense if they're talking about one of those two pluralities.

MR. RAVEL: It's -- it's one of the devices, not one of the pluralities. It modifies something different which I should have made more clear because that's the heart of the argument.

THE COURT: Okay. Then I'm -- I didn't follow what you just said so help me out.

MR. RAVEL: Can I approach?

THE COURT: Of course.

MR. RAVEL: The, the plurality of interrupt storage devices.

THE COURT: That's just repetitive of what's said in the first line of each of the other paragraphs.

MR. RAVEL: Right.

THE COURT: Maybe Mr. Lee can help.

MR. RAVEL: I think Mr. Lee can explain what I'm trying to say better.

THE COURT: I think that'd be great.

MR. RAVEL: And I'm happy to defer.

MR. LEE: Very quickly, Your Honor.

THE COURT: Sure.

MR. LEE: When it says one of the plurality, it's one of the plurality of interrupt priority storage devices. So the one of is not one of the plurality. It's one of the devices if you read on in the claim. And up here it's a plurality of interrupt storage devices, a plurality, and then this is the

plurality that's the search of the antecedent basis. I was trying to whisper in Mr. Ravel's ear because I think when Your Honor focused on one of, it's not one of the pluralities. It's one of the devices.

THE COURT: I understand. Let me -- in fact, let me just -- what will help -- what's unfortunate is where the slide cuts off. So let me just look at this.

MR. RAVEL: You selectively couple the device, not the plurality, Judge.

THE COURT: Okay. Thank you, sir.

Yes, sir.

MR. HATTENBACH: All right. I don't think the fact that it's going to device as opposed to a plurality of devices is anything we either disagree with or that affects the analysis that Your Honor was articulating. It goes back to the example with the apples or, if you like, maybe I should have used the word "fish" since the plural of fish is fish just like the plurality of plurality is plurality. That was hard to say.

If I said, I'm going to provide you with some fish and then I'm going to provide you with some fish that have big scary teeth and I say, you need to select one of the fish, everyone would know what we were talking about. And that's all that's happening here.

I did have a moment to look for the answer to Your Honor's other question about our Slide 307, and the answer I think is

yes. On our opposition brief we said on Page 40, in any event, if the Court finds that the claim would benefit from clarification, it can easily be clarified through interpretation in the manner VLSI proposes. And then in our reply brief we said on Page 19, quote, Claim 1 requires at least one plurality of interrupt priority storage devices, itself made up of at least two such devices. So we did change the word "made up" to "comprised." Happy with either one of them, but that's the concept that the claims we're trying to get across, and, again, we think the worst case scenario for this claim should be it should be chided for being too wordy and it should be clarified or left alone.

Thank you, Your Honor.

THE COURT: Anything else, Mr. Ravel?

MR. RAVEL: No, Your Honor.

THE COURT: Thank you, everyone.

With respect to the following claim term, the Court is going to find that it is not indefinite. We will take under consideration whether or not it deserves a claim construction as suggested by plaintiff, but I don't -- I don't know whether that's likely or not, probably not likely, but it's not out of the question that we'll get you a claim construction, but for purposes of today's hearing, I find it's not indefinite.

Is there anything else that we need to take up?

MR. LEE: Not for Intel, Your Honor.

THE COURT: Counsel?

MR. HATTENBACH: Not for VLSI, Your Honor, other than to say thank you for your time. I know you put a lot of effort into this and we appreciate it.

THE COURT: Well, and I don't know how many clients are here. I recognize at least Intel has a client here which I always think is the very best thing that can happen. I think it's important for not only the lawyers who appear in front of me but for their clients to be here and have some idea of who their case is in front of and whether that's a good thing or not. But I will say, without any reservation, this -- you guys are all exceptional. I truly think I have the greatest job on the planet, and the reason why is I have the most amazing lawyers on the planet arguing things and I just hope I lived up to the high standard that each one of you had in terms of the preparation of your briefs and your arguments here today. You all made every single decision that I had to make very difficult because the arguments on both sides were so strong and well written and argued. So I thank you all for being here. I am probably -- well, I'm certain I'm unlike most other federal judges, but I am probably most different in that I am the person who is least interested in seeing you guys settle. I think this -- it would be tremendous to have a trial. I think settlements are great. I think cases should settle because I think that's just a good thing for America and for

05:33 everyone involved if you can resolve it, but I'm very much looking forward to every phase of this case up through and, if it happens, including trial. So I very much appreciate everyone being here.

05:34 We're close to Christmas. I wish everyone a merry Christmas and happy new year and I look forward to seeing you all when we get back together.

05:34 THE BAILIFF: All rise.

05:34 (Hearing adjourned at 5:34 p.m.)

UNITED STATES DISTRICT COURT)
WESTERN DISTRICT OF TEXAS)

I, Kristie M. Davis, Official Court Reporter for the United States District Court, Western District of Texas, do certify that the foregoing is a correct transcript from the record of proceedings in the above-entitled matter.

I certify that the transcript fees and format comply with those prescribed by the Court and Judicial Conference of the United States.

Certified to by me this 20th day of December 2019.

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